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# A MICROPROCESSOR-BASED SWITCHING POWER CONVERTER TEST BED

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# FOREWARD

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# CHAPTER 1

# INTRODUCTION

Power electronics is the study of electronic circuits for control of large amounts of power, far beyond the device ratings. The power electronics era [1] started with high-power tubes such as thyratrons, ignitrons and mercury arc rectifiers. With the advent of power semiconductor devices such as SCRs, triacs and transistors, power electronics has found widespread application [2] in the electrical and computer fields. Some examples include the computer industry [3], aerospace industry, electronic equipment industry, electric power industry [4], and industrial controls. Today, power electronics is being offered as a separate course in many universities [5].

As each area of technology in the electronics industry evolves, it is more often than not accompanied by the development of a succession of new circuits. Each new circuit appears different, employs different components in different configurations, and claims an assortment of distinct features of "improved performance." Without a considerable investment of laboratory time and effort to construct, evaluate and compare each candidate circuit, it is usually difficult to realistically appraise the relative merits of one approach over another. It is often even more difficult to identify the underlying principles which point up basic similarities and differences. Such is indeed the situation in the expanding area of electronic power processing or switching mode power supplies [6].

## 1.1 Need for a Generic Power Converter

It is almost universally accepted that new concepts or designs for switching power converters must be scrutinized in depth through experiments. The necessary breadboarding

effort requires many iterations and is time-consuming and expensive. Details are sufficiently important that relatively minor changes require a complete set of new experiments. In the distant future, circuit simulation will replace most breadboard steps. This is taking place in the VLSI area. However, in power electronics, detailed experimental confirmation will be needed at all levels of design for the immediate future.

The need for detailed experiments has been an impediment to novel circuit technologies and control design techniques in power electronics. For example, while many hundreds of alternative topologies have been proposed for dc-dc conversion [7, 8], few have been subjected to the necessary experimental scrutiny. In the control area, new methods are typically tested on only one or two simple circuits.

There is a clear need for experimental systems which allow the necessary data to be obtained quickly and at a minimum cost. Such a system would need to be flexible enough to test a wide range of topologies. It would need to be able to implement almost any conceivable control method. It should be able to perform "real" conversions at practical power levels. Such an experimental test bed controlled by a microprocessor is described in this thesis.

The remaining part of Chapter 1 presents a brief background on switching power converters and the switch matrix. The concept of microprocessor-based control is introduced, followed by a summary of the merits and limitations of such a control.

Chapter 2 gives a literature survey of previous generic test beds. In particular, three different approaches are reported and their limitations summarized. The advantages of actual experimental results as compared to circuit simulation are emphasized. The salient features of the new test bed approach are presented.

Chapter 3 characterizes the specific criteria that need to be considered when designing and constructing such a test bed. The design is divided into three different stages, and the requirements of each stage are considered separately. The functional features of the test bed are reviewed.

Chapter 4 describes the actual design and operation of the test bed. The actual circuit diagrams and specific hardware details, the software, and a concise manual for the test bed as built are presented in the appendices.

Chapter 5 illustrates some experimental results produced with the test bed. Typically expected results are displayed as confirmation. Conclusions are summarized.

## 1.2 Switching Power Conversion Circuits

The application of switching power supplies has been spurred by the need for power sources of higher performance, smaller volume and lighter weight to achieve compatibility with the shrinking size of all forms of communication and data handling systems, and particularly with the portable battery-operated equipment in everything from home appliances and hand tools to mobile communication equipment. Switching converters provide interfaces with new direct energy sources such as solar cells, fuel cells and thermoelectric generators, and form the central ingredient in most uninterruptible power sources. Such solid-state power conditioners operating with internal frequencies of tens to hundreds of kilohertz are emerging as the new mainstay of most power supplies for computers and communication systems, a role they have played over the last two decades for the space programs of the world.

Almost all of the power electronic circuits utilize power semiconductor switching devices [9] which ideally present infinite resistance when off, zero resistance when on, and

which switch instantaneously between those two states. These switches, coupled with lossless energy storage elements such as inductors and capacitors, and electronic control circuitry, form the basis of a power electronic circuit. The control circuitry determines the switching function for the switches and hence the type of power conversion required. A basic switching power conversion system, then, consists of some input energy source, some output load and a power electronic circuit for conversion [10, 11], as shown in Figure 1.1.

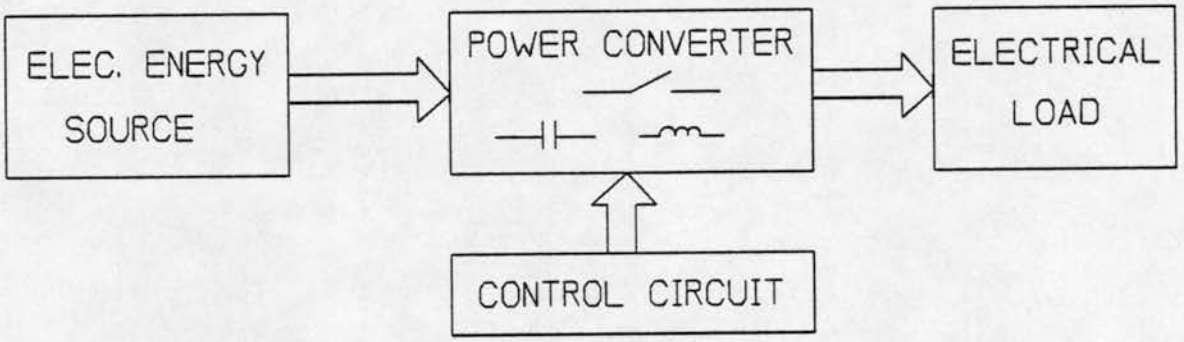


**Figure 1.1 A Basic Power Electronic System**

The conversion is performed in accordance with the Kirchoff's voltage and current laws.

## 1.3 The Switch Matrix

There are four basic power conversion functions that can be implemented:

- ac to ac
- ac to dc
- dc to ac
- dc to dc

Within each conversion function lies the possibility of a great variety of converter topologies and implementations. If a converter topology is postulated to implement the most

general function, that is, polyphase ac to polyphase ac, then the converter topologies capable of implementing all other functions can be derived therefrom. The topology postulated to fulfill the most general function is called the *general switching matrix*; all other converter topologies can be derived from it by applying appropriate functional restrictions leading to topological simplifications.

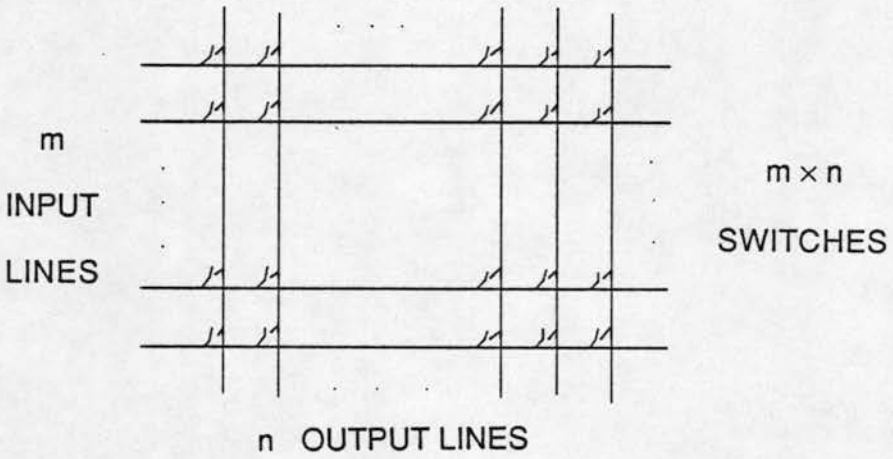


**Figure 1.2 The General Switch Matrix**

The general switching matrix depicted in Figure 1.2 represents the simplest conceivable switching converter topology that can perform the polyphase ac to polyphase ac conversion function, comprising a single switch placed, for example, at each intersection of the m input lines and n output lines. The densest possible circuit would have at most a single switch between any input line and any output line.

Following are some of the points to be kept in mind when using the concept of a general switch matrix:

a. Kirchoff's voltage and current laws restrict switch operation for proper power conversion.

b. Power flow is bidirectional between input and output.

c. The wanted output frequency depends solely on the switching pattern; it is independent of and may be lower than, equal to, or higher than the input frequency.

d. Appropriate variation of the switching pattern can produce any wanted output level from zero to the crest value of the input.

e. The matrix can be viewed as a generalized transformer, since it can transform frequency, phase angle, and, within stipulated limits on maximum output voltage and input current, impedance.

f. The matrix comprises bilateral power switches, that is, the switches must be able to carry current in either direction, when closed, and to support the voltage of either polarity, when open. They could be closed and opened in a repetitive pattern, on command.

g. The output quantities depend on the input quantities and the switching pattern. The existence of unwanted harmonics (or frequencies) in the dependent quantities is an inherent and inevitable consequence of the use of switching, as opposed to linear power converters. Although they do not generally participate in the power transfer process, they usually limit a switching converter's performance and application, and play a primary role in the design of interfaces.

### 1.3.1 Mathematical representation

Each of the switches in the switch matrix is either on or off at a particular instant of time. The condition of the switches indicates the operation of the converter. This can be represented mathematically by the *switch state matrix* $S(t)$, which is a rectangular matrix with $m$ rows and $n$ columns. Each element $s_{ij}(t)$ in this $m \times n$ matrix is associated with the switch at the physical location $(i, j)$ in the switch matrix. The element $s_{ij}(t)$ has a value of 1 whenever the associated switch is on, and a value of 0 when this switch is off. The

elements of $S(t)$ are time-varying functions with values of 0 or 1. They are referred to as *switch state functions*, or simply as *switching functions*.

The switching function is a convenient tool to describe the operation of a switching converter circuit. It builds up a design framework for creating a desired conversion operation. Taking the Fourier series approach, the switching function can be considered as a simple periodic square wave with a particular frequency. It can have one of only two values : 1 or 0, hence is a square wave when plotted. A pulse train of arbitrary period $T$, with one pulse centered on the time $t=t_0$ is shown in Figure 1.3. Each pulse has a time width $DT$, where $D$ is the *duty cycle* or *duty ratio* ($0 \le D \le 1$).

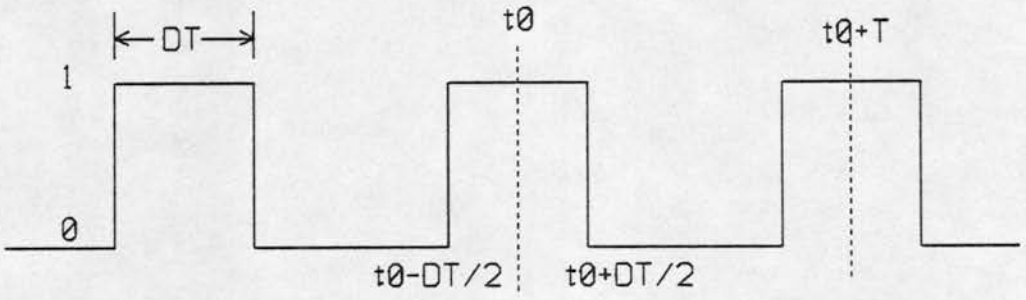


**Figure 1.3 A Periodic Pulse Train**

If this switching function is labelled as $h(t)$, then the Fourier series for $h(t)$ is

$$h(t) = D + \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{\sin(n\pi D)}{n}\cos(n\omega t - n\phi_0)$$

The Fourier analysis shows that the function $h(t)$ is determined completely by only three parameters : the duty ratio $D$, the radian frequency $\omega=2\pi f$ (or the period $T$) and the reference time $t_0$ (or the reference phase $\phi_0$). It can be used to formulate piecewise-sinusoidal representations of power electronic converter waveforms. It can be controlled with pulse width control, pulse width modulation, phase control or phase modulation. It

must have a Fourier component at the sum or difference of the desired input and output frequencies.

### 1.3.2 Half-bridge inverter example

To understand the application of the switching function in converter analysis, consider a half bridge inverter, with a dc voltage input and an ac current output.

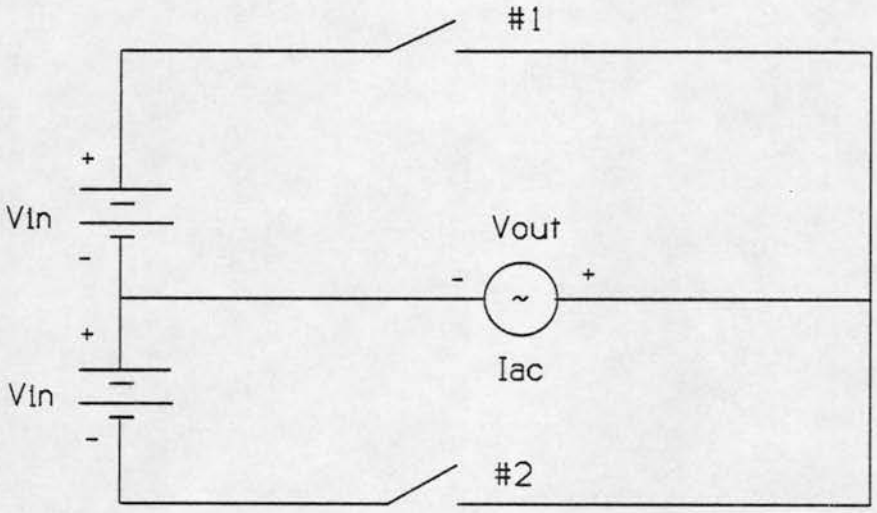


**Figure 1.4 Half-Bridge Inverter**

If the two switches are operated in a complementary fashion, then $h_1(t) + h_2(t) = 1$. In addition if the switching function duty ratios are made to vary sinusoidally with a frequency of $\omega_{out}$ (wanted output frequency), proper control can be obtained.

Let $D = ½ + k\cos(\omega_{out} - \phi)$, where $k$ is an arbitrary gain factor. To hold the duty ratio between 0 and 1, the condition $0 \le |k| \le ½$ has to be satisfied.

The output voltage then turns out to be

$$\begin{aligned} V_{out}(t) &= h_1(t)\cdot V_{in} - h_2(t)\cdot V_{in} \\ &= (2h_1(t)-1)V_{in} \\ &= 2kV_{in}\cos(\omega_{out}t-\phi) + \frac{4V_{in}}{\pi}\sum_{n=1}^{\infty}\left\{\frac{\sin[\frac{n\pi}{2}+n\pi k\cos(\omega_{out}t-\phi)]}{n}\cos(n\omega_{sw}t-n\psi)\right\} \end{aligned}$$

This is termed PWM (Pulse Width Modulation). To understand PWM, consider a very fast square wave. The duty cycle can be varied slowly (relative to the switching frequency) between 0 and 100%, in a manner similar to pulse width control in dc-dc converters. If this slow change is sinusoidal, the average value of $V_{out}(t)$ will change sinusoidally also (in two quadrants). The parameters involved are the switching frequency $\omega_{sw}$, the modulating function frequency $\omega_{out}$, the switching function phase $\psi$, and the modulating function phase $\phi$. It is well-known that the lead term can be isolated and the others filtered away if $\omega_{sw} > \omega_{out}$. The amplitude of the output voltage is controlled by changing the modulating gain $k$.

## 1.4 Microprocessor-Based Control

Clearly, switching power conversion circuits can be constructed and implemented with switch array circuits, organized in a matrix fashion. A particular conversion objective is achieved by specifying appropriate switching action. The switch matrix yields a more direct picture of the effort needed for power electronic design. There are two major problems to address:

The *hardware* problem : Build a switch matrix

The *software* problem : Control the switching action in the matrix to achieve the desired conversion

Indeed, on having built the required switch matrix, the desired power conversion is achieved purely by controlling the switching action. Thus, conversions in all four quadrants of the voltage-current axes can be achieved if the switches are operated properly. Today, intelligent switching control action is implemented easily with the advent of microprocessors. Since the beginning of 1970s the microprocessor has brought a new dimension to power electronics and drive technology. The impact of this evolution is as

significant as the advent of power semiconductor devices in the 1950s. The implementation of microprocessors has not only brought about simplification of hardware and improvement of reliability, but also permitted performance optimization and powerful diagnostic capability which were not possible before in dedicated hardware control. The performance of microprocessors in terms of functional integration, improvement of architecture and speed of computation has continually improved since their introduction at the beginning of 1970s, a trend that will continue [12].

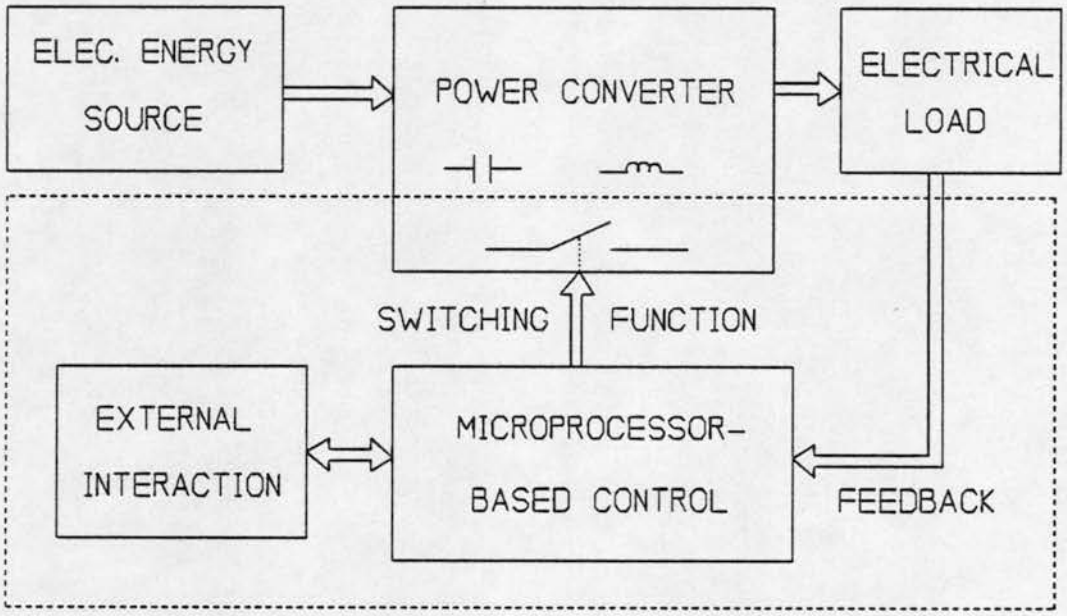


**Figure 1.5 Microprocessor-Based Control for Switching Power Conversion**

The concept of a generic switching power converter controlled by a microprocessor is thus framed easily [13]. A simplified block diagram of a microprocessor controlled switching power converter is shown in Figure 1.5. The test bed would essentially consist of the blocks shown inside the dashed line. The hardware being universal, any type of power conversion in any of the four quadrants can be achieved purely by software, given a

bilateral switch matrix. The switching action, which is highly nonlinear by nature, can be controlled and implemented through appropriate software.

### 1.4.1 Merits and limitations

The microprocessor or, in general, the digital design of a control system, has some merits and limitations which can be summarized as follows [14] :

*1. Low Hardware Cost*

Custom or semicustom VLSI chips with integration of total control hardware for a specific application in a large volume production can be very economical. Smaller size and less weight with reduced power consumption are the additional advantages.

*2. Improved Reliability*

System reliability or MTBF (mean time between failures) of an LSI or VLSI chip is higher than that of an electronic circuit with a large number of electronic components.

*3. Fewer EMI (Electromagnetic Interference) Problems*

VLSI minimizes coupling of large voltage and current transients in a power electronic system.

*4. No Drift and Parameter Variation*

Digital signal processing eliminates signal drifts and parameter variation effects which are prevalent in analog controllers.

*5. Universal Hardware and Software*

Universal hardware can be designed for systems in which software can be modified to satisfy the subclass specifications.

*6. Diagnostics*

Powerful diagnostic software whose implementation need not necessarily require skilled personnel can be designed. Data acquisition, signal monitoring, warning, and displays can be provided.

*7. Sluggish Computation*

Most microprocessors have rather limited analog conversion and computational capabilities, although the new generation of digital signal processing integrated circuits is helping somewhat in this regard.

*8. Quantization Error*

A finite quantization error occurs when analog systems are interfaced with a microprocessor through A/D and D/A converters.

*9. Lack of Access to Software Signals*

Microprocessor control does not provide easy access to software signals for monitoring as compared to oscilloscope monitoring of a hardware controlled system.

*10. Software Development May Be Expensive*

Software development, especially in assembly language, may be very time consuming and thus expensive.

Today, microprocessors have been accepted universally in power electronics and drive systems, and the spectrum of their applications will grow continuously. In the forthcoming industrial revolution, that is, the computer automation of factories [15], offices and homes, microprocessors will play a vital role not only in higher-level supervisory control but also in lower-level control of power electronics and drive systems. Power electronics and drive technology, which is already interdisciplinary, has reached a new dimension of complexity.

# CHAPTER 2

# EXPERIMENTAL SYSTEM ALTERNATIVES

## 2.1 Circuit Modelling

Switching power conversion circuits have relatively few component parts when compared to other circuits such as communications equipment. The analysis of such circuits, however, is not as simple, except under the simplest and least interesting conditions. The switching action being highly nonlinear, the analysis becomes nearly intractable when one addresses the issue of dynamic behavior resulting from control system interactions or anomalous operating conditions. The efficacy of simplified models [16] for such cases is well-established. The type of model selected [17], however, depends on the nature of the analysis, the problems to be solved, the facilities available, and the previous experience of the investigator. Ideally, the model can serve as a design tool to test a particular circuit configuration under various operating conditions and changes in system topologies.

## 2.2 Previous Work

Precise circuit design and accurate analysis fundamentally require a one-to-one correspondence between the circuit being modelled and the actual model. The existence of such topological isomorphism allows a true "breadboard approach" to modelling. Numerous models have been reported in various journals for switching circuits [18, 19, 20, 21]. These models have assumed many forms, among which are the physical breadboard, the digital computer [22], the analog computer, and the hybrid computer.

Practically speaking, however, these models have been inflexible and expensive when applied to systems employing numerous switching elements, each of which causes a change

in system topology. The limitation of the models, when used as interactive design tools for different topologies, is apparent. Clearly, there is a need to implement a generic model which can be configured quickly at a minimum cost to test different switching power conversion circuits at practical power levels.

Previous literature has not reported much on such generic test beds, although one strong effort in this direction has been made at the Massachusetts Institute of Technology. A "parity simulator" of static power conversion systems has been designed and implemented successfully [23, 24]. Other reported models have involved dedicated hardware, oriented only to the specific type of circuit topology discussed [25]. Some others have involved pure simulation [26, 27, 28] which again has an inherent limitation of fundamentally being only a simulation as compared to actual experimental results.

The parity simulator was an early approach to the problem of a broad-based experimental tool. It was designed specifically for that class of circuits employing switching elements, such as diodes, transistors and thyristors, for the processing of electrical power. There is a one-to-one correspondence or "parity" between the circuit topology of the system being modelled and the topology of the interconnected model. Whereas the traditional modelling approaches are rather inflexible with respect to changes in system topology and limited in their interactive capabilities, parity simulation is able to provide the necessary investigator interaction along with the ability to change element values or circuit topology with relative ease. Thus, the parity simulator combines computation with live circuit elements. This is done by providing a hybrid model in which the power circuit, containing all the switching elements, is modelled using synthetic analog element modules with appropriate voltage and current characteristics, and the control system is simulated, for the

most part, on a microprocessor-based minicomputer. A block diagram of the general system is depicted in Figure 2.1.

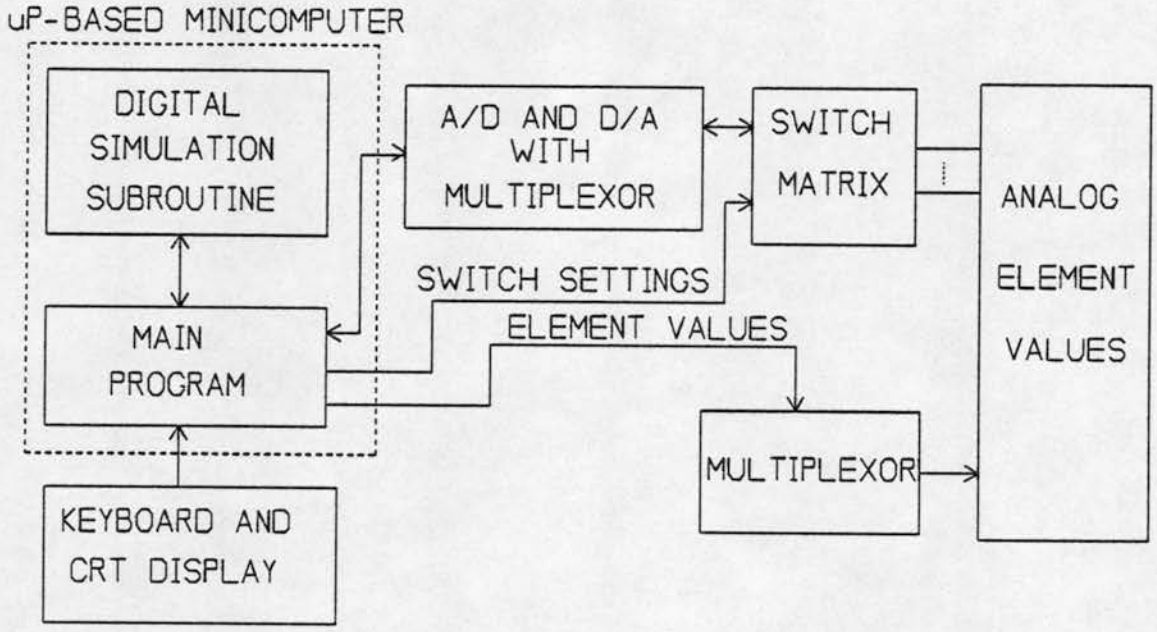


**Figure 2.1 The Parity Simulation System**

The minicomputer also provides simulation control, data processing and interactive graphics. In this way, detailed studies of waveforms and converter dynamics can be made quickly. While parity simulation in principle offers a convenient, accurate design approach, it has not been widely used. One weakness is the dedicated nature of the synthetic elements and their accuracy. Another reason is that the method is still fundamentally a simulation, and designers remain reluctant to substitute simulated results for direct experimental tests. Although in principle it can be extended to electrical networks in general, the technique begins to lose its advantages when the application strays from systems exhibiting time-varying topologies.

Another example of a generic approach to the analysis of power electronic circuits is the one developed at the University of Toronto [28]. This approach, which is suitable for

the development of general purpose simulation software for power electronic circuits with feedback control, overcomes the problems based on a state-space formulation of the circuit equations. Some of these problems include the formulation of state equations for an arbitrary switching circuit topology and the stiffness of equations.

In applying this method to a power electronic circuit, the power circuit is considered separately from the control elements. Kirchoff's current law at each node of the power circuit presents a set of nodal equations, which in turn are used to compute nodal voltages. Inductor and capacitor branches are modelled with equivalent resistors in parallel with current sources. Control loops can be represented based on transfer functions with limiters, or in terms of circuit elements and operational amplifiers. The basic structure of a nodal based simulation scheme for power electronic systems containing feedback is shown in Figure 2.2.

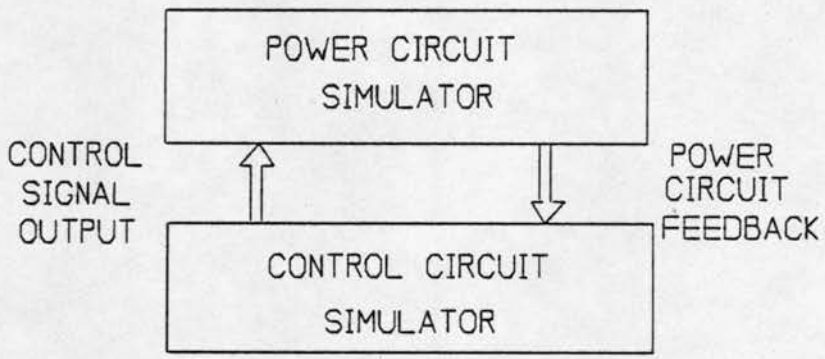


**Figure 2.2 Power and Control Circuit Modules for General Purpose Simulation**

As with most simulation software for power electronic systems, the problem is based on monitoring the states of "real" switches. An inherent difficulty with this approach is dealing with the discontinuity which occurs at switching times. Monitoring the switching devices is not very easy. The operation of all solid-state switches has to be assumed as ideal. In addition, it is assumed that every switch has an associated control signal which is always

available. Equivalent representations of inductances and capacitances might add to the complexity of an already complex power electronic circuit. The mathematical analysis of the system may prove time consuming. The transient characteristics of "real" switches are not visualized practically. And finally, the approach remains a simulation, which need not necessarily reflect an actual circuit's performance.

An effort to implement a generic setup solely for the control of electrical drives has recently been made at the University of Washington [29]. A laboratory setup for instruction and research in the control of electrical drives has been proposed. The system is assembled using off-the-shelf integrated modules. A general purpose simulation software is used to perform any desired control function. A personal computer is used to house the software and to provide adequate interface between the software and the external hardware. The controller and interface circuits are modular. The rating of the power electronic switches determines the maximum drive capability. The system can be used in high-performance drives such as robotics.

The key functional blocks of the system are shown in Figure 2.3. The main modules of the setup are: a dc motor, a power switching module, a driving module, a position encoder, and a personal computer. The terminal voltage of the motor is controlled by a PWM signal, on command from the PC. The drive circuit consists of optocouplers, buffers and the switches. Currents, voltages, speed and rotor angle are used as feedback. A software package called TUTSIM is used [30].

The setup is designed for dc drives. An ac drive will require control over the input frequency and amplitude, which in turn would require extensive additional hardware for proper three-phase control. Execution time depends to a large extent on the clock frequency of the PC as well as the number of blocks in the controller. Although the system is flexible

as far as electric drives are concerned, a practical system which can incorporate all of the above features, along with the additional ability to control power conversion in any of the four quadrants, would serve as a more general research tool.

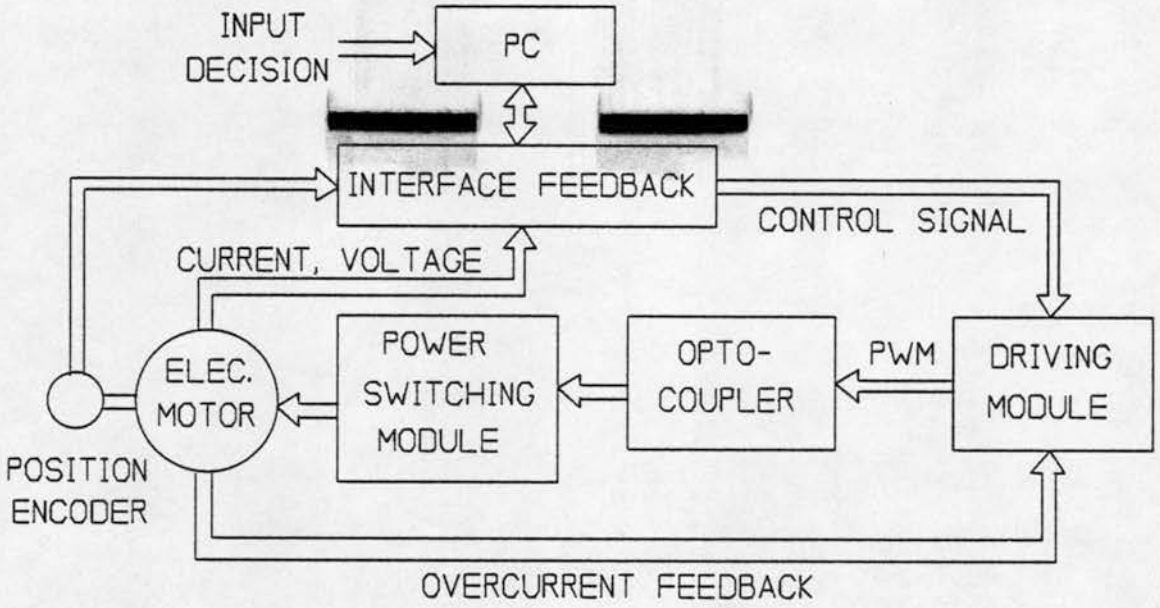


**Figure 2.3 Laboratory Setup for Control of Electric Drives**

A "patchboard" approach, based on canonical switch configurations [31, 32], could be used, but sensitivity to layout details limits the utility of this method. The need to study feedback control methods would make a patchboard system complicated and prone to error.

## 2.3 New Converter Test Bed Approach

The experimental system reported here returns to the most basic power electronic topology: the switch matrix. The control of switches requires manipulation of switching function timings and duty ratios. The new system provides these basic functions. The

objective is a generic switching converter which can be configured quickly for a given test. Such a converter can be used to evaluate switching power supply topologies, motor control techniques, new PWM schemes, and resonant converter approaches, among many other topics of current interest. A block diagram of such a system is depicted in Figure 2.4.

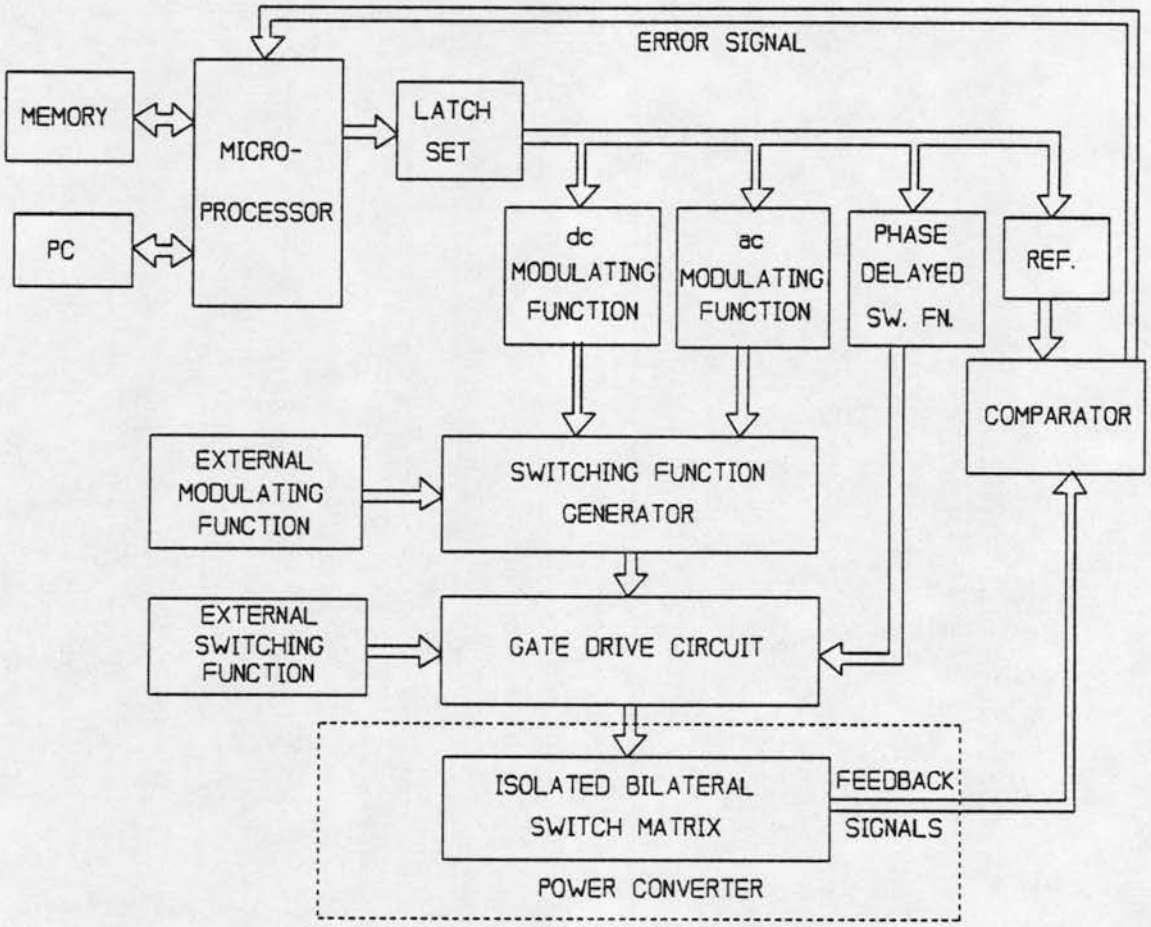


**Figure 2.4 A Generic Switching Power Converter Test Bed**

The overall design of the system is based on three different stages: the digital control circuit, the analog processing circuit, and the switch matrix with the gate drive circuit. The heart of the digital circuit is the microprocessor which commands full control of the test bed. The analog circuit appropriately processes the various digital signals and converts them to

the required modulating or switching functions. The gate drive circuit converts the modulating functions to the required switching functions which drive the switch matrix. Feedback signals from the converter are compared to appropriate references, and the error is fed back to the digital circuit to be analyzed and processed.

The system is based on universal hardware, with control provided through appropriate software signals. It provides in-depth insight into the actual performance of switching power converters and electric drives, as compared to simulations. It can be configured quickly for any converter topology. A bonus is the ability of such a system to serve as an effective demonstration tool. Early stages of breadboard evaluation become much more convenient when they can be conducted with such a system.

# CHAPTER 3

# TEST BED REQUIREMENTS

## 3.1 Introduction

Having defined the objective, it is now appropriate to understand the basic requirements and capabilities of the generic converter. The converter should possess the basic intelligence to control all four types of power conversion (ac-ac, ac-dc, dc-ac, and dc-dc). Additional capabilities could include flexibility of the system for future modifications and research. A microprocessor would function as the "brain." Commands would be converted to analog signals through an analog circuit. The final stage could include the switch matrix and the gate drive circuit for transferring the switching commands to the actual switches. Each of these stages has certain requirements and certain restrictions with respect to qualities such as function, speed, power capacity, and easy availability of components. The most important functions and the design criteria of each stage are presented below.

## 3.2 Digital Circuit Requirements

In the beginning of the microprocessor era, microprocessors were used essentially for the implementation of logic control functions, that is, as Boolean function synthesizers for programmable logic control applications. As the microprocessor architecture improved in word length, execution time, and hardware functional integration, its application gradually expanded to general control systems. The main criteria of the digital control circuit design are summarized below.

### 3.2.1 Microprocessor functions

In the experimental power electronic test bed reported here, the ideal microprocessor functions can be categorized in general as follows:

*A. Feedback Control*

The control of a power electronic system is implemented by one or more feedback loops depending on the application and performance requirements. A digital feedback control system is discrete-time in nature due to the periodic sampling of signals and the switching effect of power semiconductor devices, and it may be linear or nonlinear. The discrete-time characteristic can be neglected if the sampling and switching intervals are short compared to the system response time.

*B. Nonlinear Function Generation*

Nonlinear single or multidimensional functions can be generated by a microprocessor through a look-up table, by means of piecewise-linear approximations, or through curve-fitting techniques.

*C. Estimation of Feedback Signals*

Some feedback signals, such as voltage, current and speed can be sensed directly in voltage form and then converted to digital form through analog-to-digital (A/D) converters. Signals not easily measurable, such as torque, flux, power and power factor can be computed from the accessible signals, and the system parameters from the mathematical relations.

*D. Programmable Time Delay*

A microprocessor can easily generate adjustable time delays by software up-counting or down-counting principles.

*E. Pulse Width Modulation (PWM)*

A microprocessor can generate a PWM signal for chopper or inverter controlled drives through hardware or software counters and look-up tables.

*F. Digital Filtering*

A digital filter corresponding to a specified analog transfer function can be realized by a microprocessor.

Other functions include monitoring and warning, protection and fault overriding control, data acquisition, sequencing control, and tests and diagnostics.

### 3.2.2 Choice of the microcontroller

Once the above functions are acknowledged, the control system design is effected through a suitable choice of a microcontroller, the major considerations being the following:

*A. Speed*

Speed of execution is a compromise among required switching frequencies, accuracy, ease of programming and sampling delays for feedback control. If nothing else, the microcontroller has to be fast enough, to be able to generate either the references or the lower range of frequencies for the modulating function.

*B. Accurate Computations*

Most arithmetic computations require floating-point mathematics and this is a must for higher accuracy.

*C. Higher-Level Language of Interaction*

Many microcontrollers have to be programmed in assembly language, a tedious process. A microcontroller which allows interaction through a higher-level language would

be preferred. This might also eliminate the need to define various assembly language arithmetic routines to perform different computations.

*D. Ease of Peripheral Interaction*

Apart from having the ability to control individual bits of the I/O ports of the microcontroller, the system should be easy to connect to a keyboard or to a personal computer and a printer. The underlying requirement is easy interactive capability via appropriate software.

*E. Easy Availability*

This test bed's abilities to serve as a broad experimental tool for future research require the various components used in its hardware design to be readily available.

Other considerations for a digital circuit design involve the size and type of memory, system interrupt control signals and their priority levels, communication techniques, and bit size.

### 3.3 Analog Circuit Requirements

Depending on the speed and capabilities of the microcontroller, the digital circuit can be used directly to generate the switching function, in terms of its timing and duty ratios. However, if the high switching frequencies required cannot be produced by the microcontroller, the digital control circuit must drive external square-wave circuits, which in turn convert the relatively slow digital information to switching functions at the required frequencies. The function of the microcontroller is then to provide data for accurate modulating functions and switch timing.

It is well-known that a high switching frequency (tens to hundreds of kilohertz), as compared to the modulating frequency, helps separate the unwanted frequencies from the

wanted frequency. The use of appropriate filters can then eliminate the unwanted frequency components. The Fourier analysis of the switching function provides an accurate mathematical confirmation.

Clearly, the criteria going into the design of an analog circuit should consider the following:

*A. Modulating Function*

The system should have the ability to generate precise modulating functions which in turn are converted to switching functions at high frequency. For example, in the experimental system reported here, the microcontroller commands a certain frequency and amplitude from a three-phase oscillator included in the system. This generates reference signals for inverters and ac-ac converters.

*B. Phasing information*

The microcontroller sets up the references which are used to control the switching function timing which in turn are converted to actual switching functions through the analog circuit. Thus, phase control is implemented for use in current-sourced inverters, rectifiers, or even as phase modulation in ac-ac converters.

*C. Data Acquisition*

A fast and accurate feedback control network supporting several differential inputs with a wide dynamic range is necessary to permit closed-loop tests.

### 3.4 Switch Matrix Requirements

The number of switches in the matrix is determined by the maximum number of phases involved. Once this is decided, the fundamental requirement is that the switches be

able to be configured for any arbitrary circuit topologies and be able to be operated in any of the four quadrants of the voltage-current axes. These two criteria are summarized below.

*A. Gate Drive Circuit*

The switch matrix must be isolated from the control circuit so that the switches can be arranged arbitrarily in the power circuit. This involves the design of an isolated gate drive circuit with isolated power supplies for each switch. Switch isolation helps make almost any topology accessible.

*B. Bilateral Power Switches*

It is necessary for the switches to be able to block voltage and current in either direction [33]. This allows circuit configurations in any of the four quadrants of the voltage-current axes. Moreover the ratings of the switches, including speed, maximum voltage and current capabilities, and resistance when "on" must be chosen to permit power conversion at practical levels. The number of bilateral switches depends on the number of phases required. In the system reported here, power conversion can be performed with circuits employing up to three phases, giving a total of six bilateral switches, that is, two switches per phase. These two switches per phase have complementary switching functions.

## 3.5 Functional Features of the Test Bed as Built

The chief objective is to introduce a test bed which allows convenient experiments and demonstrations of a wide range of switching power converters and their control at practical power levels. The system thus should be able to perform control of basic power conversions such as:

*1. dc - dc*

Buck, boost, buck-boost, boost-buck, multi-quadrant dc-dc

*2. ac - dc*

Phase delay control (up to three phases)

*3. dc - ac*

Half- and full-bridge inverters (PWM, up to three phases)

*4. ac - ac*

PWM, or phase modulation (up to three phases)

Other features which can be incorporated into the system could include the ability to override or supplement the processor system. For example, each switching function could be available at a panel jack for measurement, synchronization, or even as an input to impose a specific switching function independent of the internal control arrangement.

Having gained an overview of the chief objectives and features of the experimental test bed, it is now appropriate to look into the actual hardware design details.

# CHAPTER 4

# DESIGN AND OPERATION

## 4.1 Introduction

Broadly speaking, the hardware design of the experimental test bed consists of three different blocks of circuits: the digital circuit, the analog circuit, and the switch matrix along with the gate drives. Figure 4.1 shows the overall system block diagram, which is described briefly below.

The appropriate software is transferred from the PC, via the serial interface, to the microprocessor, which then stores it in the memory. Depending on the software, the microprocessor sets up the appropriate enable signals for the data latches and stores the reference signals in them. For example, for a PWM inverter, the microprocessor stores the references for the required output frequency and amplitude in the data latches, which are then converted to analog signals through multiplying digital-to-analog converters. The different analog signals are then converted to appropriate modulating functions or phase-delayed switching functions and fed to the switching function generator or to the switches directly. The switching function generator modulates the given information at a very high switching frequency. This high-frequency switching function drives the isolated bilateral power switches in the required manner. The output of the converter can be sampled through analog-to-digital converters and fed back as a digital signal to the microprocessor which then alters the switching function accordingly. The microprocessor is not fast enough to generate very high switching frequencies by itself, hence the interface with the analog circuitry.

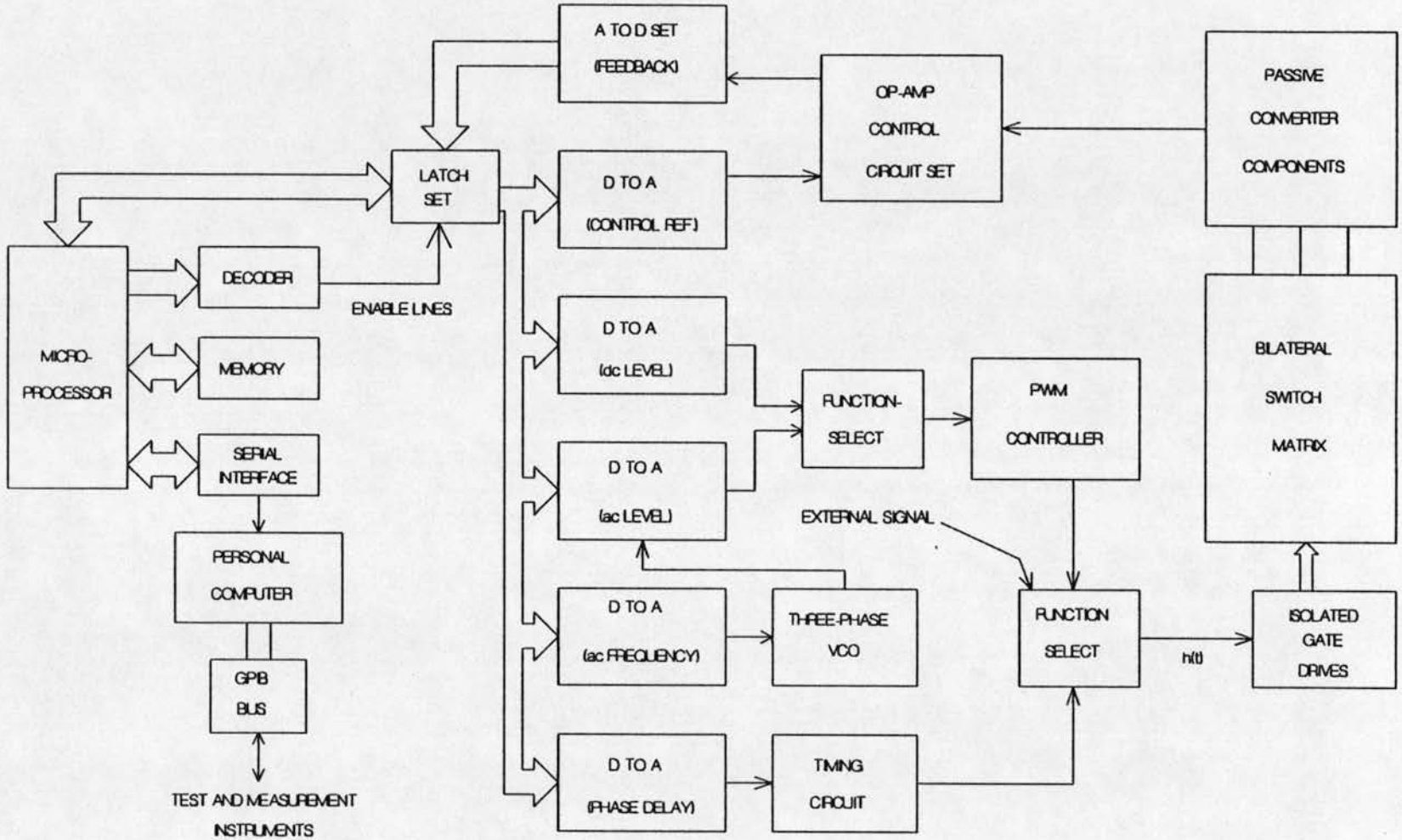


**Figure 4.1 Overall System Block Diagram**

## 4.2 The Digital Circuit

The digital circuit incorporates the microprocessor, memory, decoder circuits, data latches, and the serial interface to an IBM compatible PC.

Microcontrollers are microprocessors specially configured to monitor and control mechanisms and processes, rather than manipulate data. The systems in which they are embedded are often real-time control systems; microcontrollers always offer some form of timer structure to allow synchronization with the outside world. Some prominent microcontrollers introduced at approximately two and one-half year intervals starting in 1976, were the INTEL 8048, the Motorola 6801, the INTEL 8051 (MCS - 51), and the INTEL 8096.

The 8052AH-BASIC [34] was chosen for the system. This member of the INTEL MCS - 51 family is an 8052AH microcontroller with a complete resident BASIC interpreter. In addition to the standard BASIC [35] commands and functions, such as floating-point arithmetic and transcendental operations, the 8052AH-BASIC interpreter contains many features that allow the user to perform tasks that usually require assembly language. Bit-wise logical operators, such as AND, OR, and EXCLUSIVE-OR are supported as well as hexadecimal arithmetic. In addition, the controller can program EPROM or $E^2$PROM devices. All arithmetic and utility routines can be called from assembly language. Interrupts can be handled in BASIC or directly in assembly language. The 8052AH-BASIC is thus found suitable for the applications required.

The general block diagram of the digital circuit configuration is shown in Figure 4.2. The detailed circuit description is presented in Appendix A, Section A.1.

The software is written in BASIC or assembly language with an editor on a PC which is interfaced with the test bed. This is transferred to the microprocessor through a

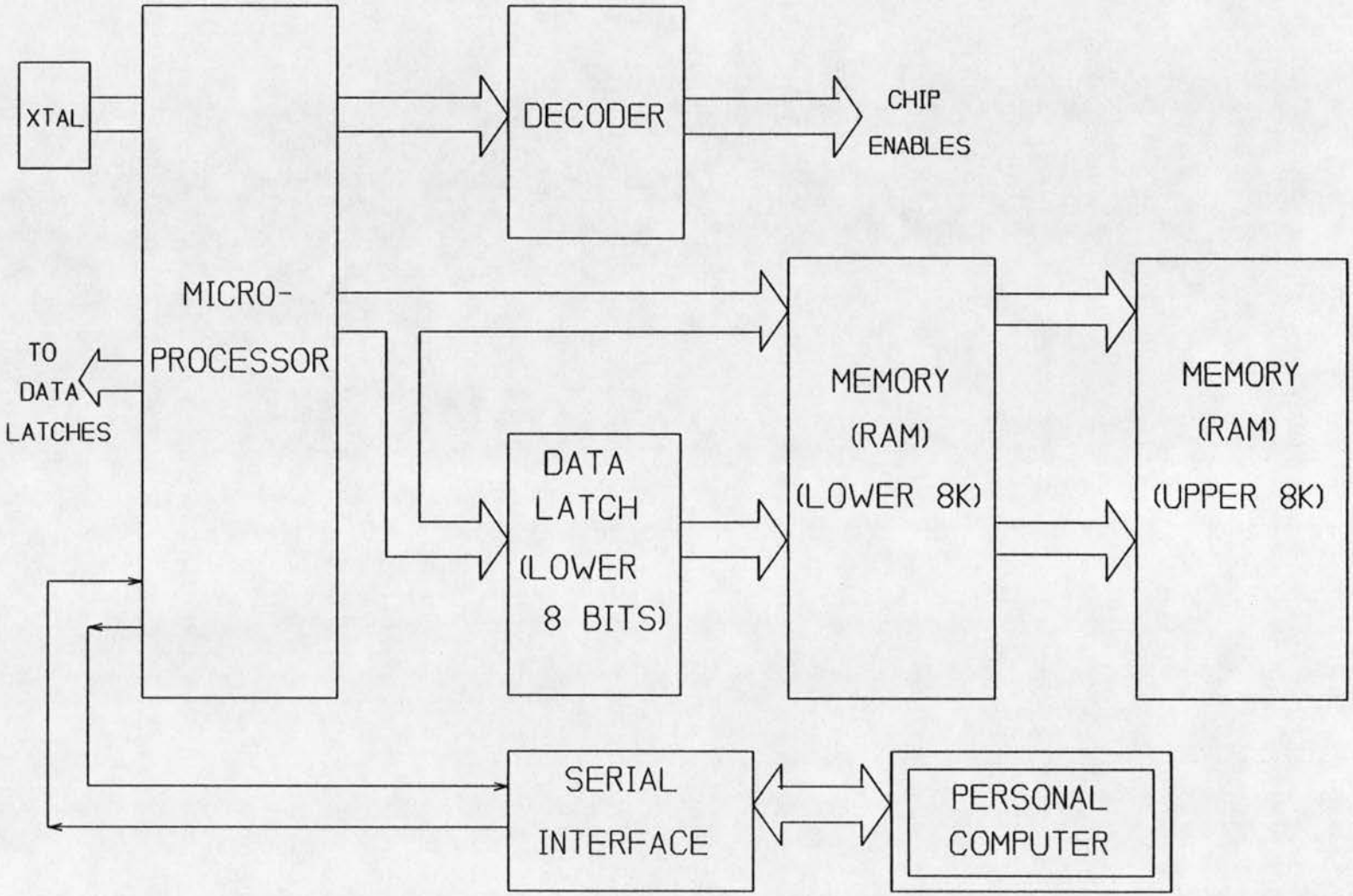


**Figure 4.2 Digital Circuit Block Diagram**

standard serial interface, with the help of a serial communications routine executed on the PC itself. Once transferred, the software is stored in the external memory. Since the 8052 is an eight-bit microprocessor, and the address bus is sixteen bits, the lower eight bits of the address are latched before data can be communicated through the data bus. Depending on the software, the microprocessor sends out various enable signals through a decoder circuit to the data latches. Once the appropriate latches are enabled, the microprocessor either stores or retrieves data from them through its input/output port. Communication with the microprocessor is done through the PC with the help of the communications routine.

### 4.3 The Analog Circuit

The analog circuit design incorporates the conversion of the references set up by the microcontroller into appropriate analog signals, which then serve as inputs to the gate drive circuit. The functions performed by this circuitry are as follows:

- generation of a dc modulating function (dc-dc).
- generation of a three-phase sine wave modulating function for PWM (dc-ac, ac-ac).
- generation of phase-delayed switching functions (ac-dc, ac-ac).
- generation of a low switching frequency which is the difference of the input and the output frequencies (dc-ac, ac-ac).
- feedback control.
- provision of external override for the modulating function or the switching function.

The main blocks for the analog circuit stage are shown in Figure 4.3. This stage essentially converts the digital control signals to appropriate switching or modulating functions. Power supplies rated at (+15 V, 1 A), (-15 V, 1 A), and (+5 V, 1 A) are sufficient for the full system.

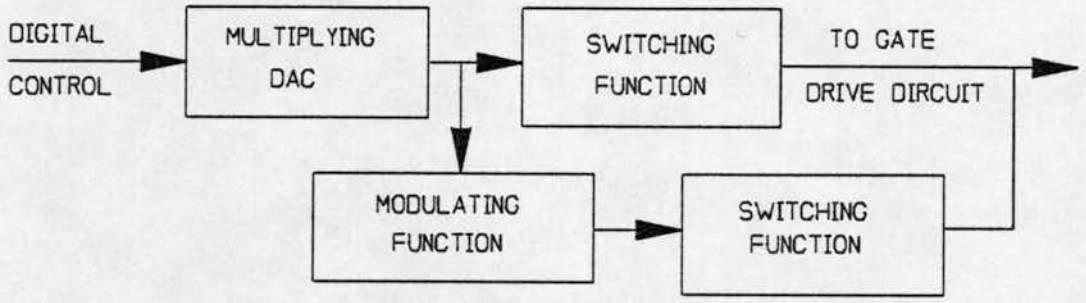


**Figure 4.3 Analog Circuit Stage**

### 4.3.1 The dc-dc conversion

Pulse width control is the basic technique for performing and controlling such a conversion. The general two-input, two-output switch network has four switches, and will provide dc-dc conversion if a dc source is used at the input and pulse width control is used to operate the switches. Multi-quadrant dc-dc converters have applications in motor drives.

Pulse width control is achieved by varying the duty ratio of the switching function. A common way to achieve this is to compare a triangle wave to a dc voltage as shown in Figure 4.4.

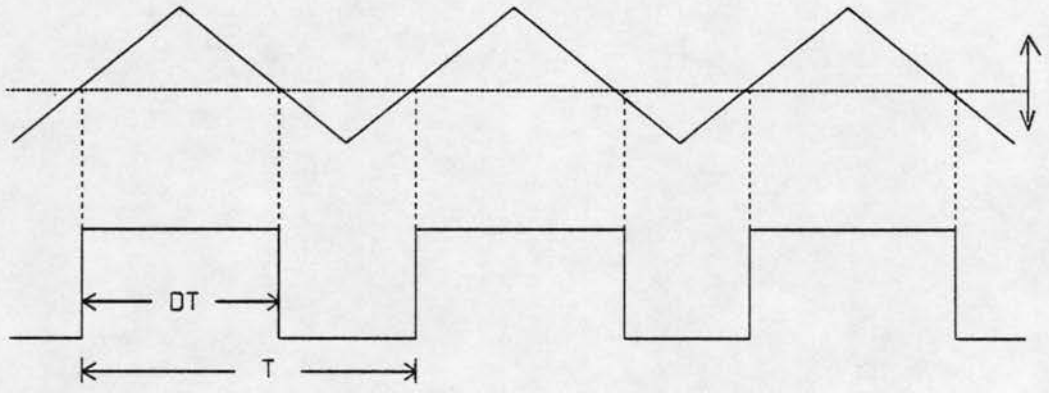


**Figure 4.4 Pulse Width Control**

If, for example, the triangle wave is higher than the dc level, the output is high, else it is low. Thus, the duty ratio $D$ is varied by varying the level of the modulating function, which is a dc level. The frequency of the triangle wave determines the switching frequency.

In this experimental setup, a switching function generator generates the triangle wave at the required switching frequency and compares it to the modulating function. The output is the switching function, which is isolated, amplified, and fed to the gates of the switches. This is described in Section 4.4. For this particular switching function generator, the triangle wave varies between +1 V and +3 V. Hence the modulating function has to be maintained between those limits for a full range of control of the duty cycle. The switching frequency is controlled by an external knob available on the front panel.

The objective then, is to generate a dc modulating function which can be varied within the specific limits of +1 V and +3 V, through software. Figure 4.5 gives a general idea of how to achieve this.

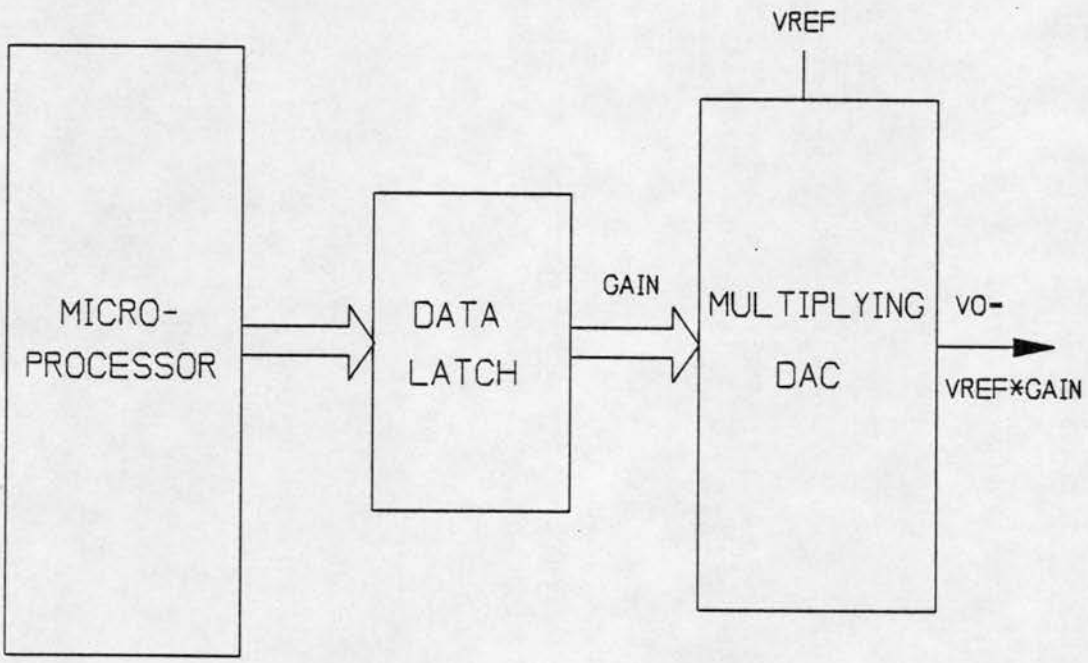


**Figure 4.5 Block Diagram for dc Modulating Function**

The microcontroller specifies a reference for the duty cycle. This reference is loaded in the data latch, when enabled. Once the reference is stored, the microcontroller can perform other functions. This reference is then converted to an analog signal via a multiplying digital-to-analog converter (DAC). This is the dc modulating function. The detailed design and operation of this circuit are described in Appendix A, Section A.2.1.

### 4.3.2 The ac-dc conversion

Phase control is the basic technique for performing and controlling such a conversion, also known as rectification. The switching function is made to have a phase delay with respect to the ac input. The phase delay depends on the required dc output. In phase control, the switching function frequency equals the input ac frequency. The frequency of the switching function is set equal to the ac input frequency. The duty cycle of the switching function is set based on the number of phases, so as to provide, for example, a maximum possible dc output value for a given reference phase value. The relative phase values depend on the number of input phases. The one remaining variable to be set is the reference phase (delay) with respect to the ac input.

Figure 4.6 shows a general block diagram for the generation of the phase delay pulses for one phase. Similar circuits generate the switching functions for the other two phases. The microcontroller software specifies the appropriate digital value of phase delay. This value is loaded into the data latch and then converted to an analog signal through a multiplying DAC. At the same time the actual ac input to the converter is converted to a square wave through a voltage comparator. The rising and falling edges of this square wave are then used to trigger two different timers. Once triggered, the timers give a high output after a certain delay. This delay is determined by the phase delay analog signal and a *RC*

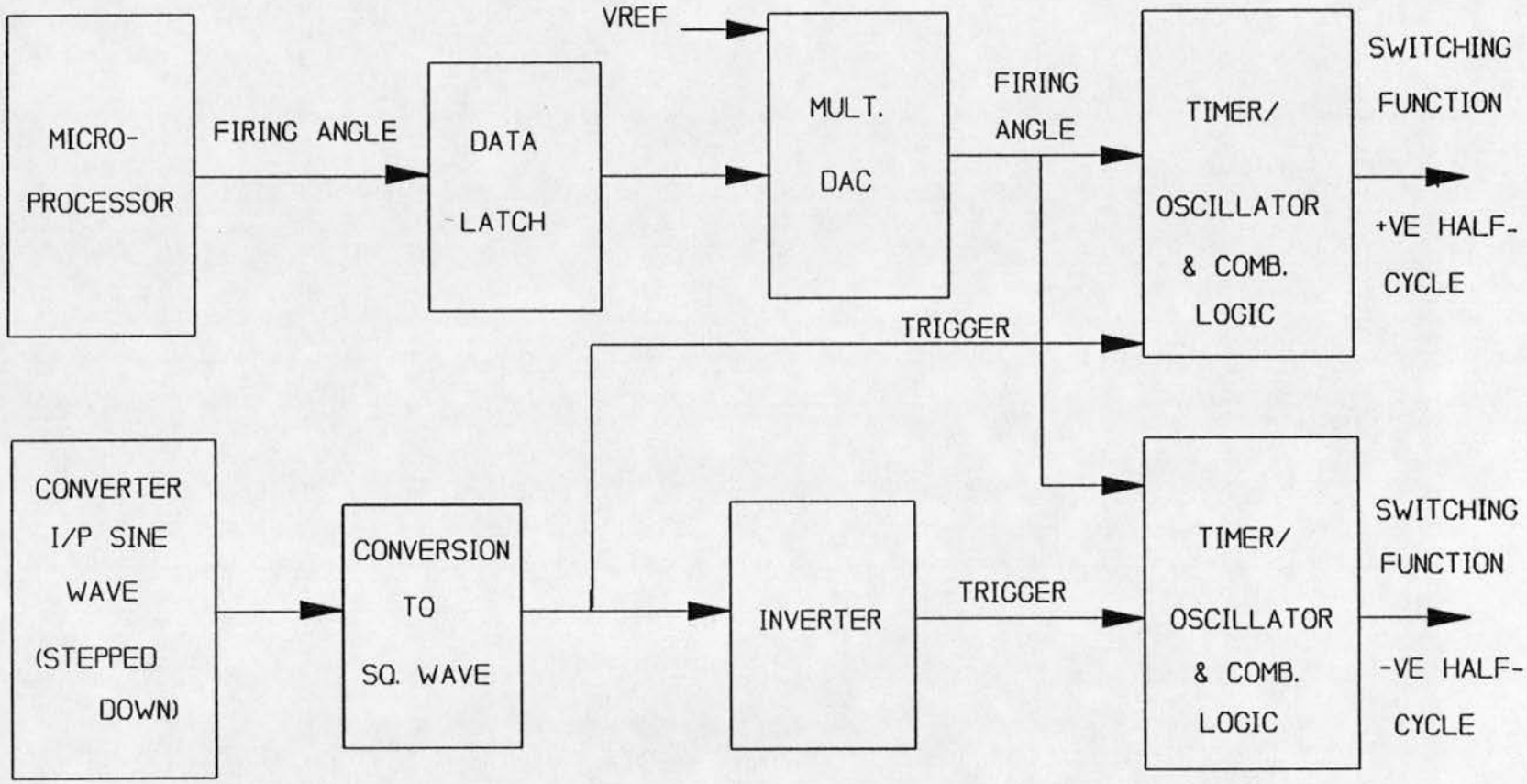


**Figure 4.6 Block Diagram for Generation of Phase-Delayed Switching Functions**

pair. The value of $C$, which depends on the ac input frequency, is set manually by a rotary switch on the side panel.

The outputs of these two timers do give a certain phase delay for the rising edge of the switching function in both half cycles, but not for the falling edge. Hence, these outputs could be used for pulse width control, or possibly, phase delay control, for example, in ac regulators.

To obtain a true phase delay for single-phase rectifiers, the two timer outputs are used to trigger and reset a third timer. This creates a switching function which has a duty cycle of one-half, a frequency equal to the ac input frequency, and a phase delay controlled by software. For three-phase rectifiers, the outputs of all single-phase timers are processed through combinational logic to create a three-phase switching function of a frequency equal to the ac input frequency, a duty cycle of one-third and again, a phase delay controlled by software. The detailed circuit design and operation are described in Appendix A, Section A.2.2.

### 4.3.3 The dc-ac conversion

Inverters, or dc-ac converters, are used for the generation of backup power, ac motor drives, alternate energy applications, dc motor regeneration and switching amplifiers. They are classified according to the properties of the dc source. Those with dc current sources can control power flow by phase control, if a fixed phase reference frame in the form of an ac voltage source is available. Those involving dc voltage sources use either phase displacement control [11] or pulse width modulation (PWM) for controlling the flow of power. The PWM inverters are quickly becoming the method of choice and their use is likely to expand. Advantages include the ease with which the wanted component of output voltage, $V_{out(wanted)}$, can be varied, the fact that adjusting the output frequency, $f_{out}$, is as easy as adjusting

$V_{out(wanted)}$, the simplicity of PWM systems, and the possible wide frequency spread between the wanted and the unwanted frequency components.

Pulse width modulation involves the intentional slow variation of pulse width at the wanted frequency. This can be done sinusoidally (sinusoidal PWM), or in any other periodic manner. This experimental test bed is capable of performing sinusoidal PWM through the microcontroller. This is achieved by comparing a sine wave to a triangle wave, as shown in Figure 4.7.

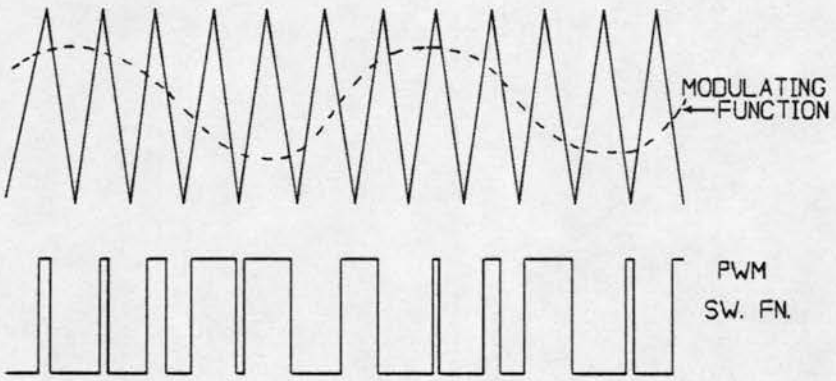


**Figure 4.7 Sinusoidal Pulse Width Modulation**

Thus, if the modulating function is varied sinusoidally and compared to a triangle wave at the switching frequency, the required PWM signal is produced. The example in Section 1.3.2 showed how this could be used to vary $V_{out(wanted)}$ and $f_{out}$. For a three-phase output, a three-phase sinusoidal modulating function is required. Figure 4.8 gives a general block diagram to produce a three-phase sinusoidal modulating function, that is, three independent sine waves. The block diagram of the three-phase function generator is depicted in Figure 4.9.

The microcontroller specifies the references for the frequency and amplitude of the ac sinusoidal modulating function. These are then loaded into their respective data latches.

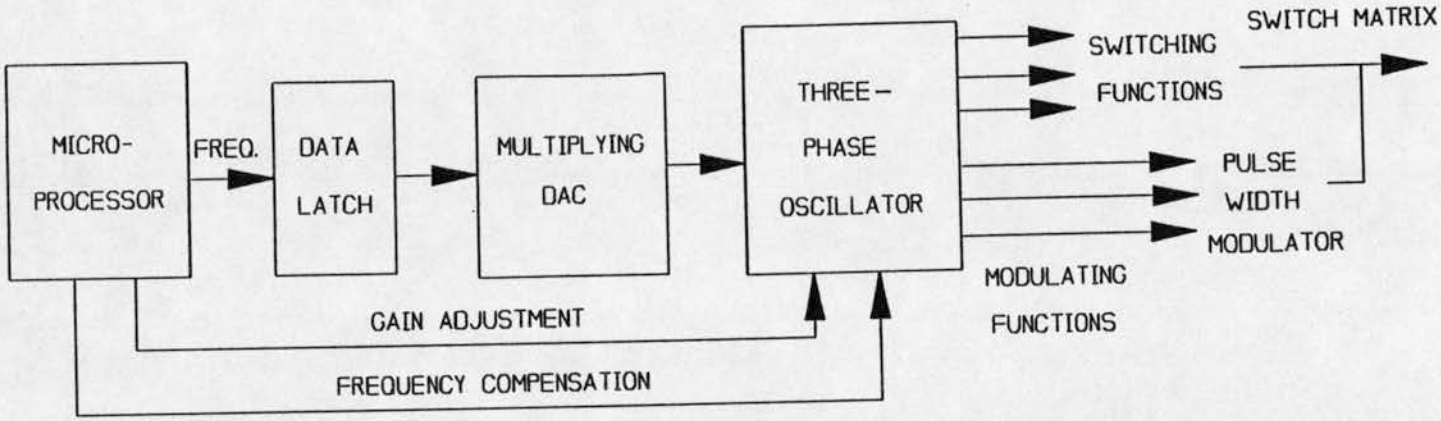


**Figure 4.8 Block Diagram for Generation of ac Modulating or Switching Functions**



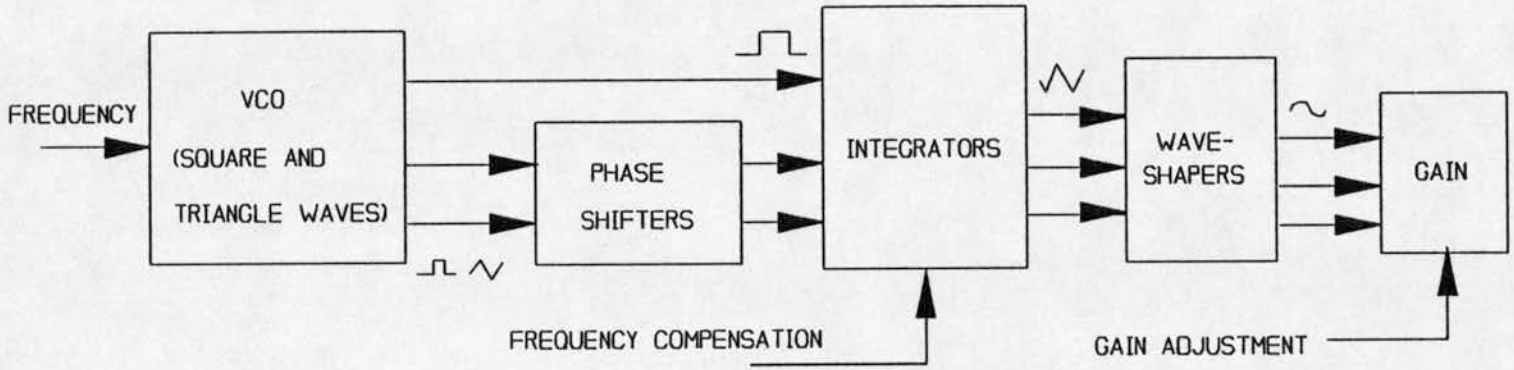


**Figure 4.9 Block Diagram for a Three-Phase VCO**

The digital reference value for the frequency is applied to a multiplying DAC. The analog output of this DAC is connected to a standard voltage controlled oscillator (VCO). This VCO generates a triangle and a square wave of fixed amplitude but with controllable frequency. These two waves can be processed through operational amplifier and voltage comparator circuits to produce three-phase square waves or two-phase square waves displaced from each other by 120° or 90°, respectively. Each wave is converted to a sine wave as follows:

The single-phase square wave is integrated to a triangle wave. The integration is frequency dependent. To provide a constant output amplitude at all frequencies, the microcontroller calculates the required digital value for the appropriate gain. A latch and a multiplying DAC set then divides the integrated triangle wave by this gain and outputs a triangle wave with a constant amplitude at all frequencies. Diode waveshaping techniques are then used to convert this triangle wave into an approximate sine wave. In the final stage, the microcontroller specifies the digital reference for the sine wave gain through another multiplying DAC. The final output is thus a sine wave of the desired amplitude and frequency. Three such circuits for the three phases produce a three-phase sine wave, which is then used as the ac modulating function. The detailed design and operation of each of these circuits are discussed in Appendix A, Sections A.2.3.1 through A.2.3.5.

### 4.3.4 The ac-ac conversion

A real ac-ac converter is a true four-quadrant device. A generic ac-ac unit would serve for any possible conversion function, including rectification and inversion. An ac-ac converter would help reduce switching network complexity and make it possible to extend ac-ac conversion into such areas as power amplifiers, if power could be converted directly from the ac mains. A true high-power bilateral switch is needed for such a conversion.

Given a bilateral switch, some of the ways in which to operate an ac-ac converter are listed below.

- set the switching frequency at either the sum or the difference of the input and the intended output frequencies.
- phase modulation (linear, nonlinear).
- pulse width modulation (PWM).

Each method has its own advantages and disadvantages. In this test bed, all of the above are possible and have been discussed previously. The first method requires that switching functions contain a Fourier component at a frequency $f_{sw}=f_{in}\pm f_{out}$. Section 4.3.3 describes the production of three-phase square waves of desired frequency, up to about 1.4 kHz. These waveforms can be used directly as the switching function, if the required switching frequency is less than 1.4 kHz. They are connected directly to the optocouplers in the gate drive circuit. External rotary switches select the function required.

The second method employs linear or nonlinear phase modulation. The above technique was an example of linear phase modulation and could be used, for example, in universal frequency changers or slow switching frequency changers [36]. Nonlinear phase modulation techniques allow control of power flow even with passive loads, for example, in cycloconverters [11]. An arrangement is provided in which an external triangle wave, approximating a nonlinear function of the form $\cos^{-1}(\cos(\omega_{out}t))$ can be connected to a panel jack to modulate the phases and drive the switches accordingly. This is described in Section 4.3.2, where an external SPDT switch manually selects whether the phase delay is specified by the microcontroller or externally. In the future, connections could be made directly, such that the triangle waves produced (Section 4.3.3) by the analog circuit could be connected to the phase delay circuit after appropriate gain and offset adjustments. The external jack

actually allows any function to modulate the phase delay, provided it is within the limits of 0 to +15 V.

The last method involves PWM. A sinusoidal PWM technique is described in Section 4.3.3 for dc-ac conversion. The same technique applies here also, where the frequency of the sinusoidal modulating function is the required output frequency. In fact, the external front panel rotary switch, which selects the conversion function, has the same sinusoidal modulating function connected in its positions for PWM (dc-ac and ac-ac). Other types of PWM are possible by applying external modulating functions or external switching functions, as described in the Section 4.4 for the gate drive circuit.

### 4.3.5 Feedback circuit

As mentioned earlier, switching power conversion is nonlinear. Fast and precise control is necessary to maintain the closed-loop stability of switching power conversion circuits. This is possible if a fast microcontroller is used. One possible type of feedback arrangement is described here.

Figure 4.10 shows the general block diagram of the feedback circuit. The basic principle is that the microcontroller sets up a reference which is converted to an analog signal. This is compared to different signals from the output of the converter through a master operational amplifier. The difference of these is converted to digital form. This digital error signal is then fed to the microcontroller, which modifies the switching function, and hence the power converter output, accordingly. This form of feedback technique is not as fast as would be possible. A faster approach is possible if the interrupt facilities available on the microcontroller are used.

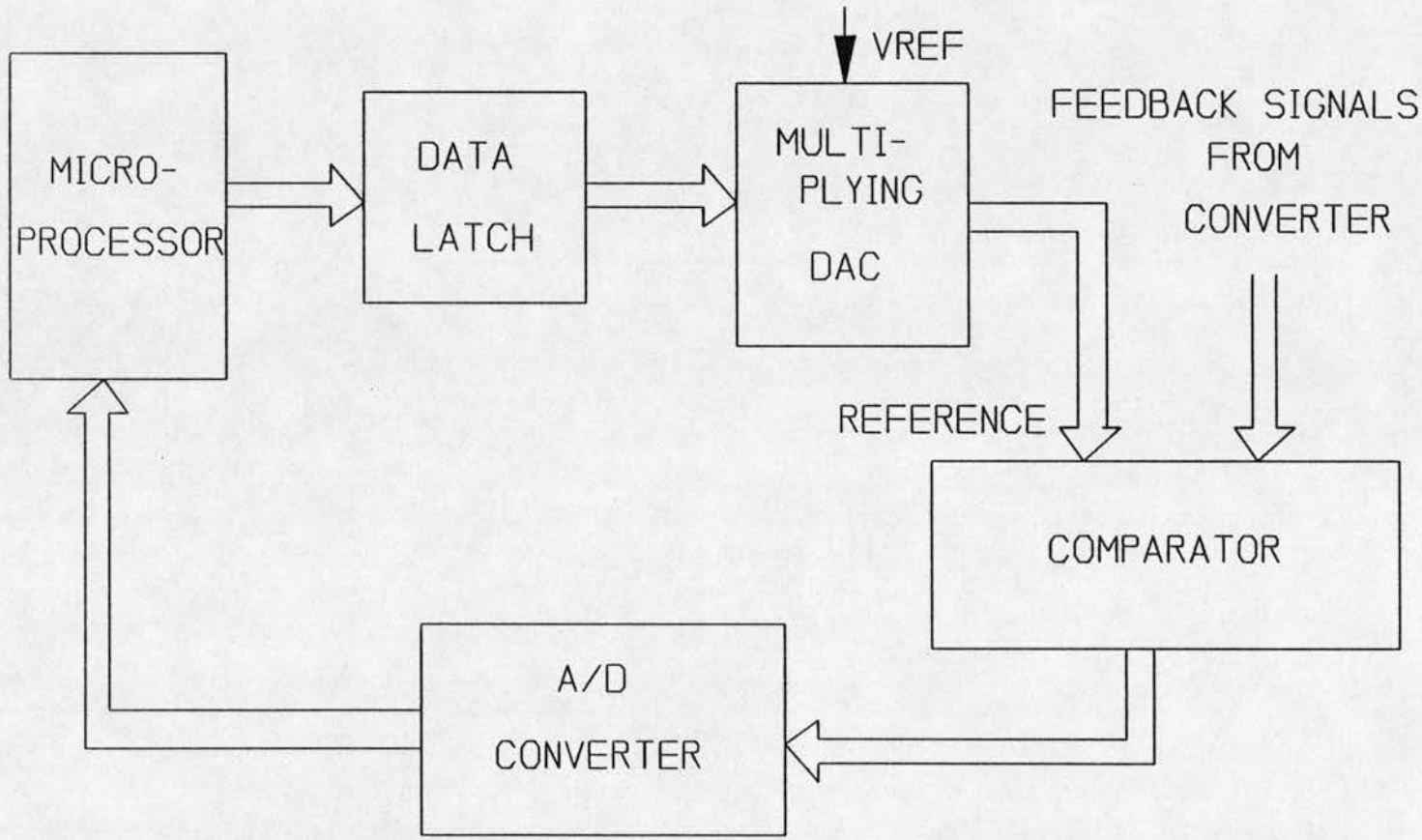


**Figure 4.10 Feedback Circuit Block Diagram**

Another form of feedback, termed the "Status Monitor," is also incorporated into the hardware for future applications. The circuit can be used, for example, to monitor the status (on/off state) of the switches. The same terminal jacks which were used in the previous form of feedback are tapped for input to four differential voltage comparators. For example, consider the operation of one of these comparators when attached across a switch in a switching power converter circuit. If the switch is on, the voltage across the switch is near zero, hence the output of the comparator is low. If the switch is off, there is some voltage present across the switch, with a value which depends on the switching circuit configuration. Hence the comparator output is high. This data is latched and fed to the microcontroller. The detailed circuit designs and operation for both these forms of feedback are described in Appendix A, Section A.2.3.6.

Thus, different feedback configurations are available, and depending on the need, faster configurations could be implemented in the hardware by using the interrupt pins of the microcontroller. The system is flexible as far as future modifications in the existing hardware are concerned.

## 4.4 The Gate Drive Circuit and the Switch Matrix

The gate drive circuit, along with the isolated high power bilateral switches, plays an important role in the configuration of any switching power converter circuit. Each gate drive circuit incorporates a switching function generator, an optocoupler, high-current buffer and isolated power supply, and a bilateral switch set with snubber circuits.

Figure 4.11 gives a general block diagram of the gate drive circuit for one phase. There are three such circuits for each of the three phases. The modulating function specified by the microcontroller or through an external source is applied to the switching function

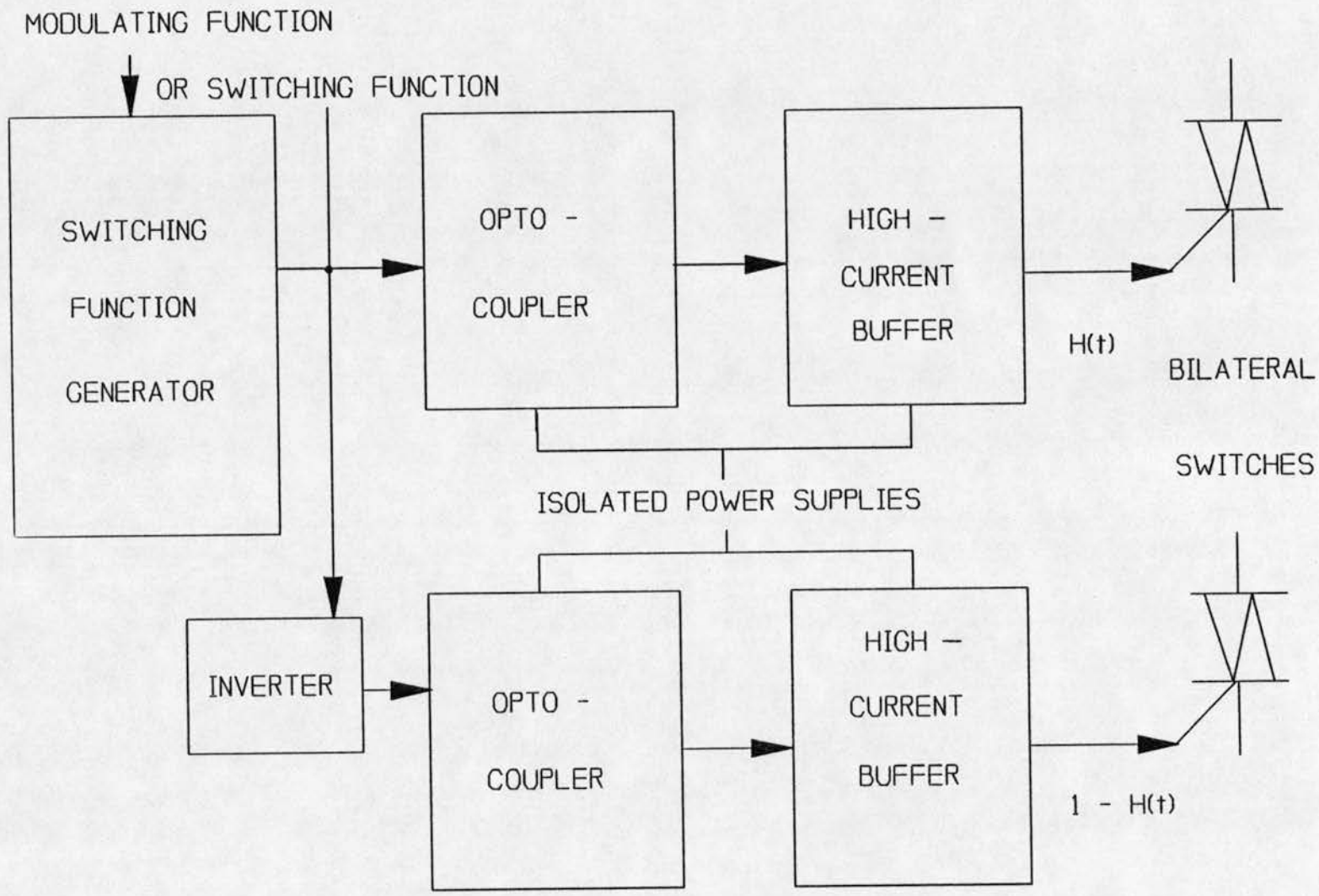


**Figure 4.11 Gate Drive Circuit Block Diagram**

generator. The switching function is then electrically isolated from the switches through the optocoupler. If the microcontroller specifies the switching function directly, or if an external switching function is available, it is applied directly to the optocoupler. For the complementary switching function, an inversion is performed and applied to a second optocoupler. Each optocoupler requires its own isolated power supply. This is implemented as a separate switching power converter. The output of the optocoupler is amplified to drive the switches. A high-current buffer is used for this purpose. The potential at the gates of the switches is clamped to avoid damage to the switch inputs. The processed switching function is then applied to the bilateral switch set.

A true high-power bilateral switch with turn-on and turn-off capabilities is not as yet available in a single package. It must be configured from discrete devices [33]. Two such switches are needed for complementary switching functions. This switch can block voltages of either polarity, conduct current in either direction, and can be turned on or off at any time. The triac approximates this device, but does not permit control of turn-off or fast operation.

Alternatively, two power MOSFETs can be placed in series to form a bilateral switch as shown in Figure 4.12.

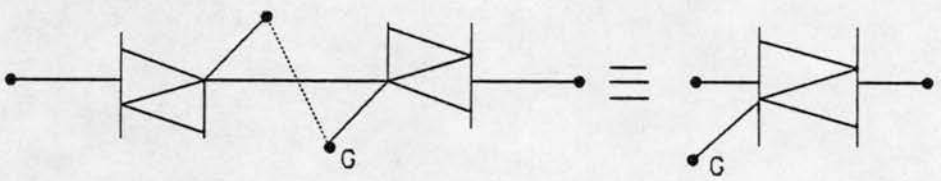


**Figure 4.12 Formation of a Bilateral Switch Using MOSFETs**

The gates of the two subunits are operated from the same switching function. The transistors chosen in this test bed can block up to 400 V or carry up to 15 A. Snubber

circuits have to be designed and connected across these switches to minimize high-voltage transients which may cause higher commutation losses or even damage the switches. The switch terminals are then available for any switching power converter configuration. The detailed design and operation of the switch matrix and the gate drive circuit are described in Appendix A, Section A.3.

### 4.5 Summary

The hardware design was described in terms of intended applications. The circuit consists of three subcircuits: the digital control circuit, the analog processing circuit, and the switch matrix with the gate drives. Each portion is described in detail in Appendix A. Figures 4.13 and 4.14 depict experimental setups for two-phase ac to single-phase ac conversion and PWM dc-ac conversion, respectively.

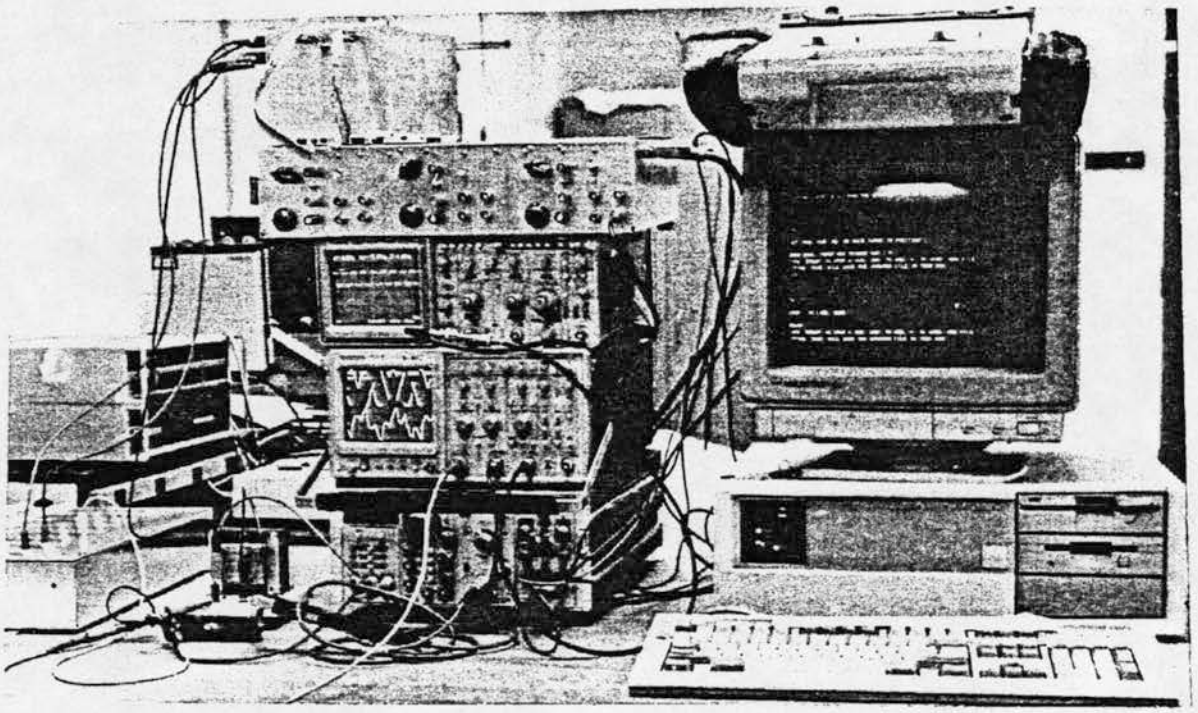

**Figure 4.13 Two-Phase ac to Single-Phase ac Conversion**

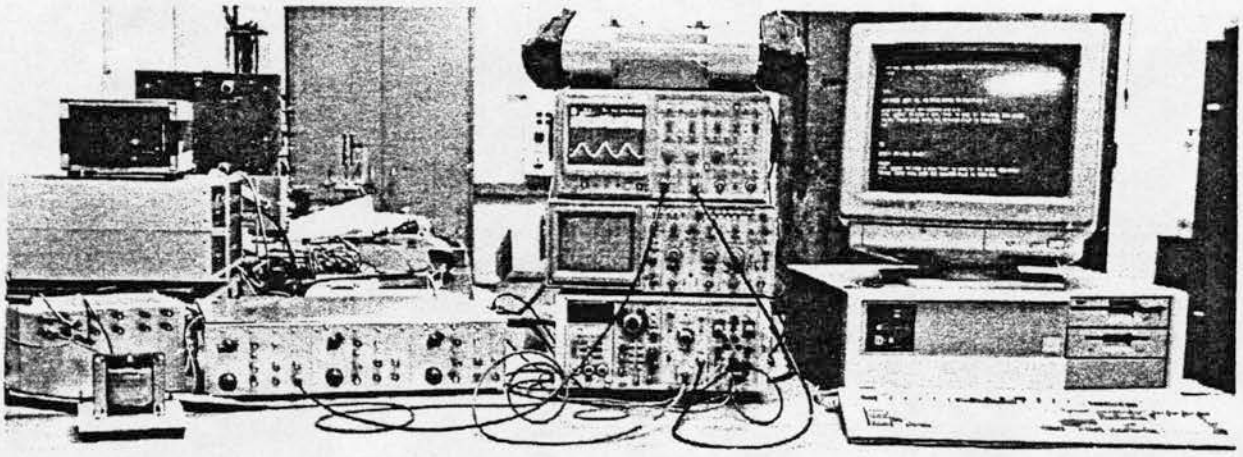

**Figure 4.14 PWM dc-ac Conversion**

The test bed is constructed in wire-wrap form and is flexible enough for future modifications and expansion. It services a total of up to three phases, involving six power bilateral switches. About 140 chips and 200 discrete parts were used in the final version. Some of the results produced for different converter tests are illustrated in the following chapter.

# CHAPTER 5

# RESULTS AND CONCLUSIONS

## 5.1 Introduction

Some results based on experiments performed with the test bed are illustrated in the following pages. These experiments are as follows:

- a single-phase controlled half-wave rectifier circuit, to illustrate phase control.
- a simple half-bridge inverter which illustrates the effect of setting the switching frequency equal to the required output frequency.
- a half-bridge inverter to illustrate pulse width modulation (PWM).
- a two-phase ac to single-phase ac universal frequency changer.
- a two-phase ac to single-phase ac slow switching frequency changer.

Software for conversions in all four quadrants is provided in Appendix C.

## 5.2 Half-Wave Single-Phase Rectifier

Figure 5.1 depicts a basic half-wave single-phase controlled rectifier circuit. The load is purely resistive. No filtering action is provided, primarily to illustrate the phase delay action. For a phase delay of $\alpha$, the expected output voltage waveform is shown in Figure 5.2. Figure 5.3 illustrates the actual input and output voltage waveforms.

The input voltage $V_{in}$ is a 60 Hz sine wave obtained from a function generator. The required phase delay $\alpha$ is specified in degrees through the software. The microcontroller then outputs the phase-delayed switching function to the bilateral switch. In this case, $\alpha$ is specified as 80°. The output waveform is consistent with the requested 80° delay as observed from Figures 5.2 and 5.3. More generally, $\alpha$ can be given any value from 0° to

180°. For three-phase rectifiers, the switches are controlled by a switching function which has a phase delay of $\alpha$ and a duty cycle of one-third.

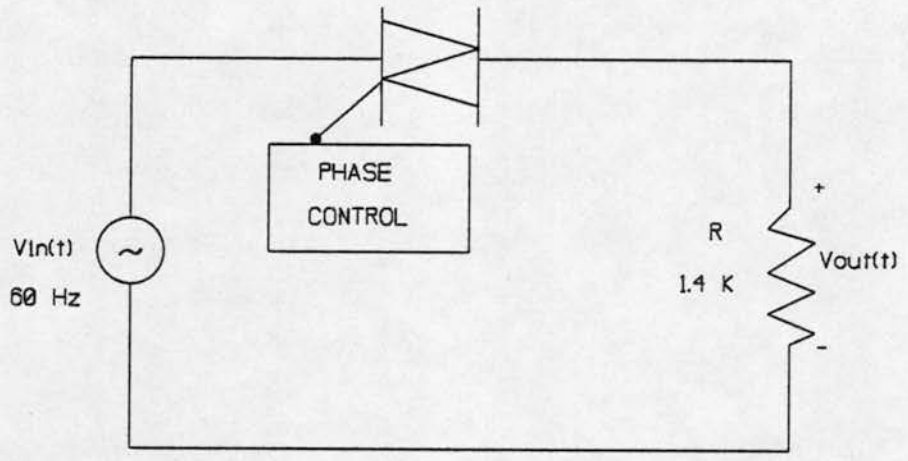


**Figure 5.1 Half-Wave Single-Phase Rectifier Circuit**

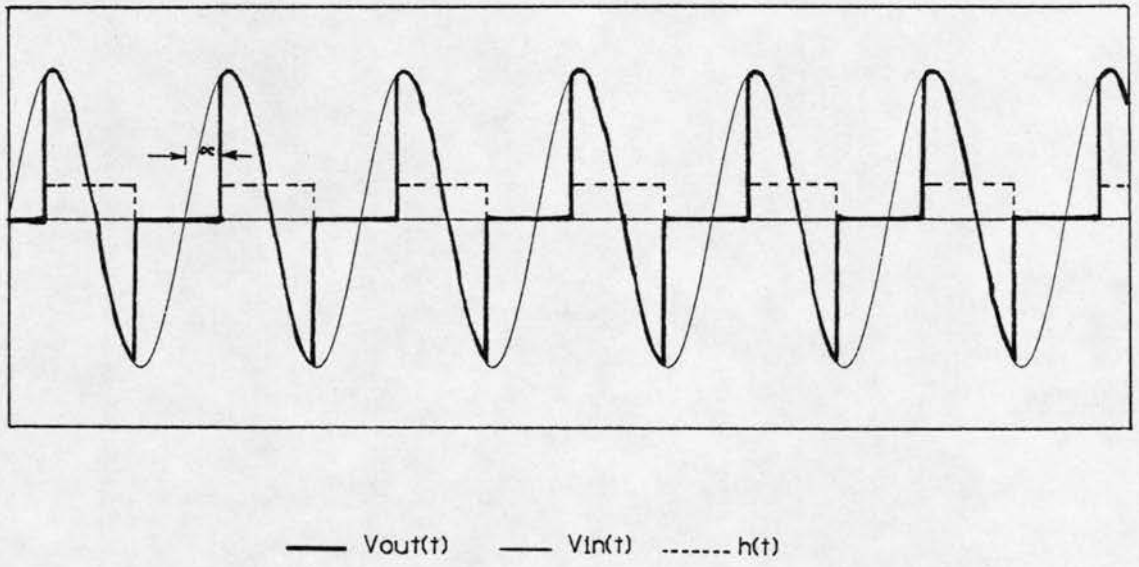


**Figure 5.2 Typical Waveforms for ac-dc Midpoint Converter**

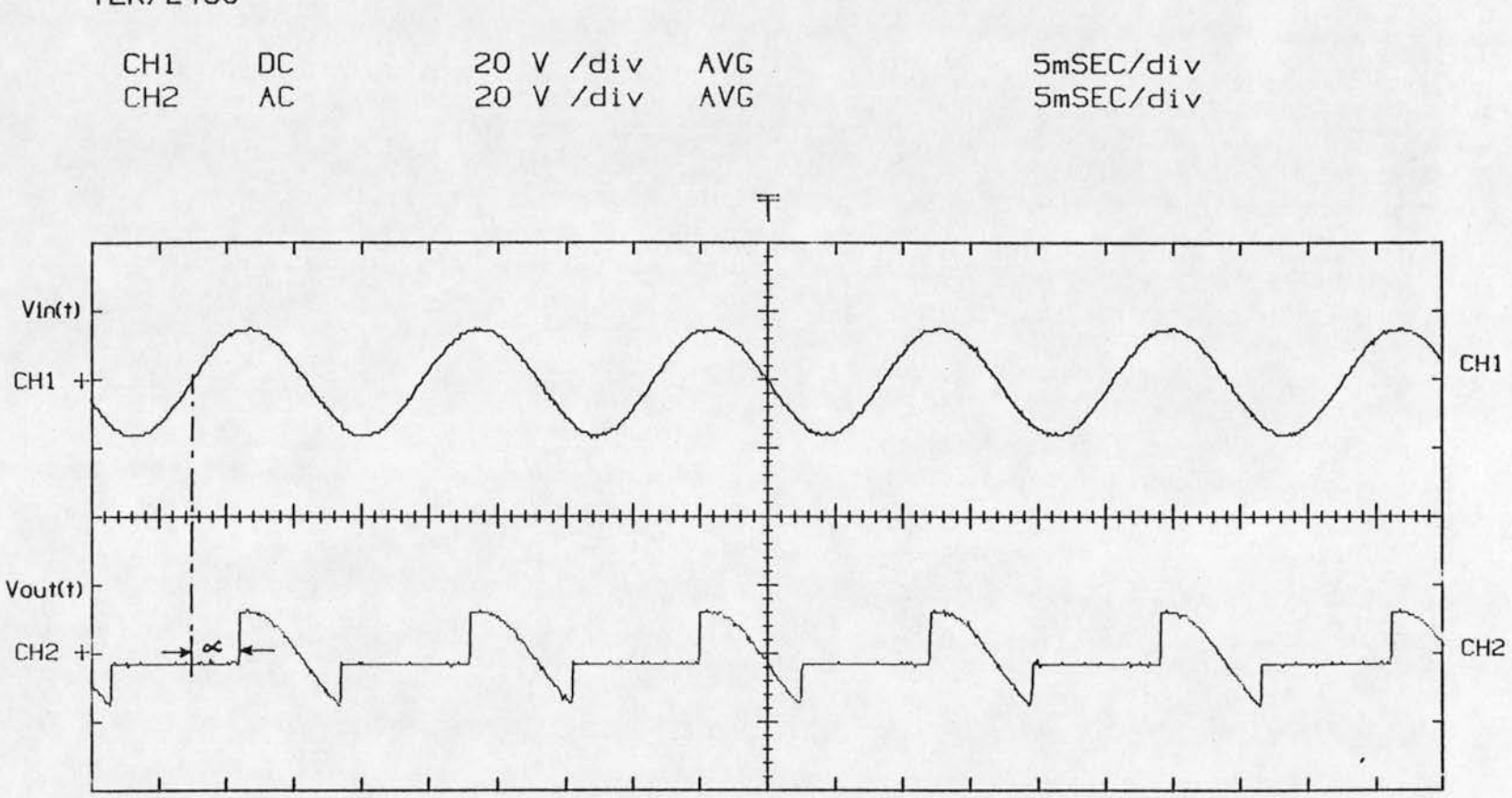


**Figure 5.3 Oscilloscope Waveforms for ac-dc Midpoint Converter**

## 5.3 Simple Half-Bridge Inverter

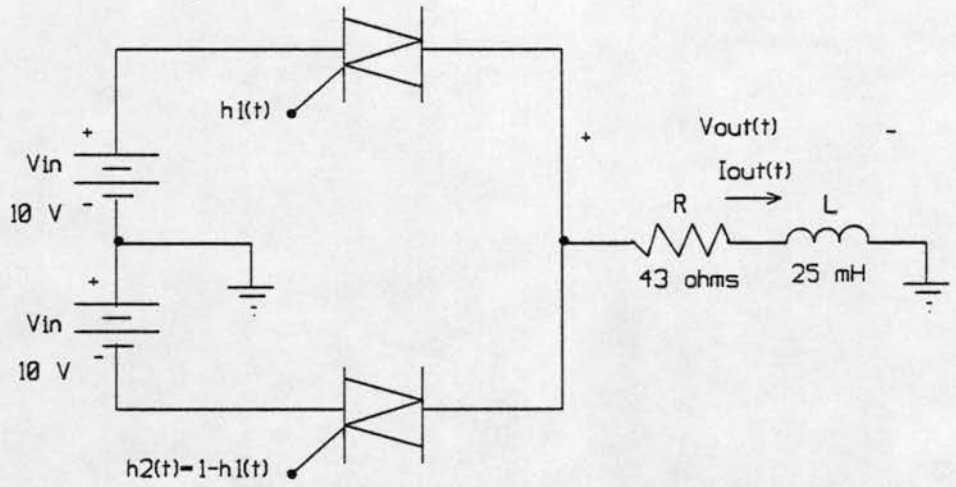


**Figure 5.4 Half-Bridge dc-ac Converter**

A dc-ac half-bridge converter with ($R$-$L$) load is shown in Figure 5.4. The results are depicted in Figure 5.5. The switching function is a simple square wave at the requested output frequency. This is generated by the microcontroller and fed to the two bilateral switches which are operated with complementary switching functions. The output voltage $V_{out}$ across $R$ and $L$ is also a simple square wave of the same form as the switching function from $-V_{in}$ to $+V_{in}$. The practical requirement of no dc component is that $D_1=D_2=½$.

$$\begin{aligned} V_{out}(t) &= h_1(t)\cdot V_{in} - h_2(t)\cdot V_{in} \\ &= (2h_1(t)-1)V_{in} \\ &= -\frac{4V_{in}}{\pi}\sum_{n=1}^{\infty}\{\frac{\sin(\frac{n\pi}{2})}{n}\cos(n\omega_{out}t-n\phi_0)\} \end{aligned}$$

In steady state, the output current $I_{out}$ is a periodic function at the same frequency as $V_{out}$. The equation for $I_{out}$ is

$$I_{out}(t) = \frac{4V_{in}}{\pi}\sum_{n=1}^{\infty}\{\frac{\sin(\frac{n\pi}{2})}{n\sqrt{R^2+X_n^2}}\cos(n\omega_{out}t-n\phi_0-\tan^{-1}\frac{X_n}{R})\}$$

where $X_n=n\omega L$.

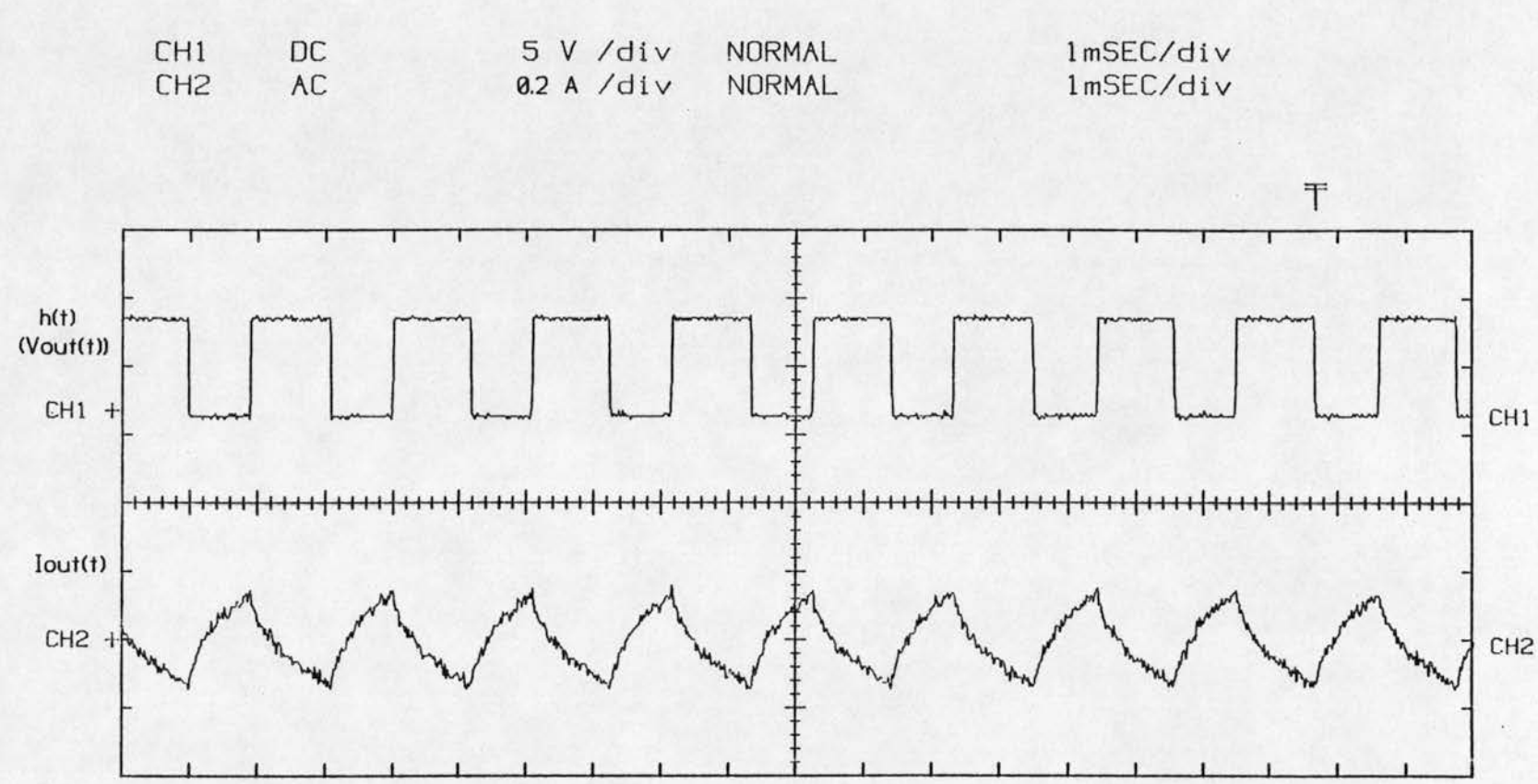


**Figure 5.5 Oscilloscope Output Waveforms for Simple Voltage-Sourced Inverter**

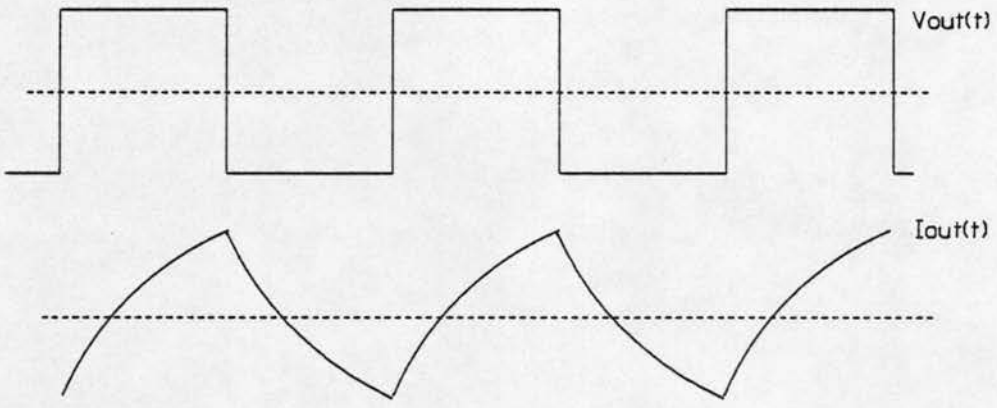


**Figure 5.6 Typical Output Waveforms for Simple Voltage-Sourced Inverter**

The expected output waveforms are shown in Figure 5.6. The input frequency being zero, the switching frequency is $f_{sw}=f_{out}-f_{in}=f_{out}$. In this particular example the output frequency is specified to be 500 Hz through software. The practical results are consistent with the theory.

## 5.4 PWM Half-Bridge Inverter

The intent of this experiment is to demonstrate the concept of pulse width modulation. The same circuit as described in Section 5.3 (Figure 5.4) is used. Pulse width modulation divorces the switching functions and their frequency from the intended properties of $V_{out}$. In this particular converter, the output frequency is specified at 60 Hz through software. The microcontroller then outputs a three-phase modulating function at 60 Hz, between the required voltage limits. This is converted to a switching function at a very high switching frequency, through the gate drive circuit. The switching frequency in this case is set at about 180 kHz. The three-phase modulating function produced by the test bed is shown in Figure 5.7.

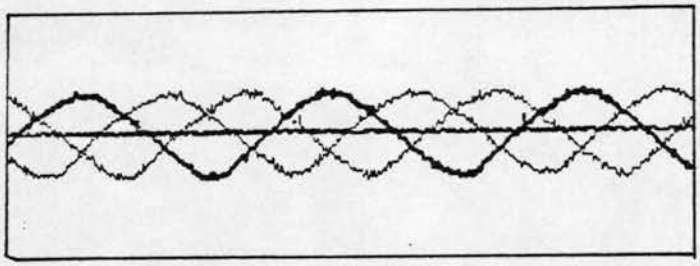

**Figure 5.7 A Three-Phase Sinusoidal Modulating Function**

Three sets of switching functions and their respective complements are thus available. One such set (phase A) is used here to drive the two bilateral switches. The circuit description is given in Section 1.3.2. Typical theoretical PWM output waveforms are shown in Figure 5.8. The results are illustrated in Figures 5.9 and 5.10.

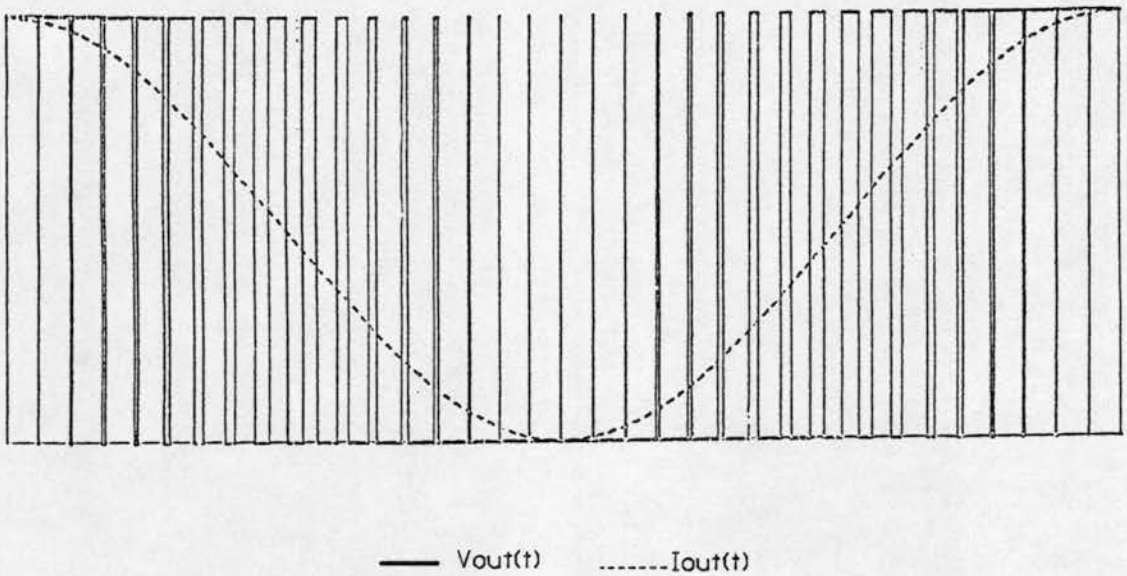


**Figure 5.8 Typical PWM Waveforms for Half-Bridge Inverter**

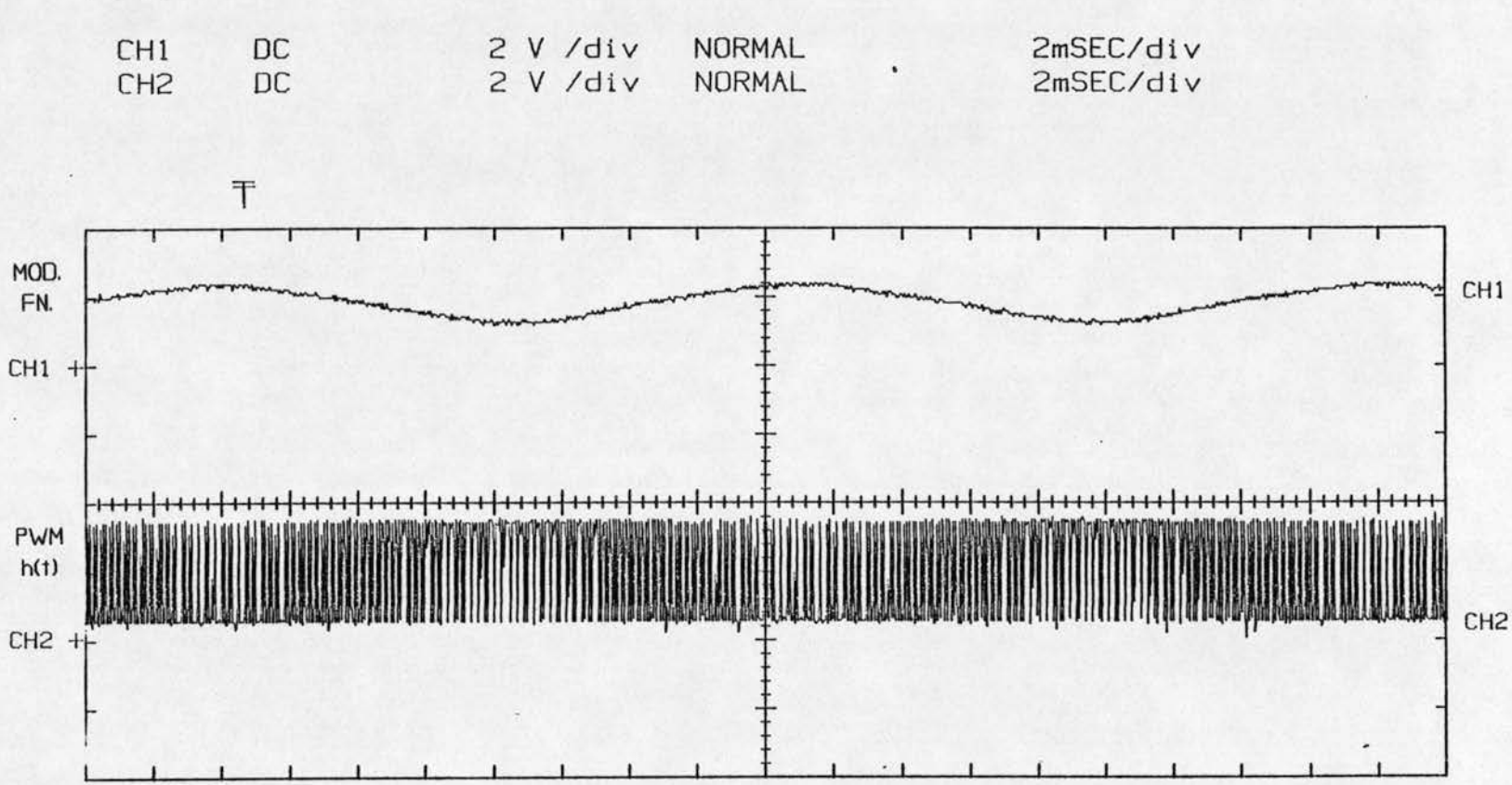


**Figure 5.9 Oscilloscope Waveforms for PWM Half-Bridge Inverter**

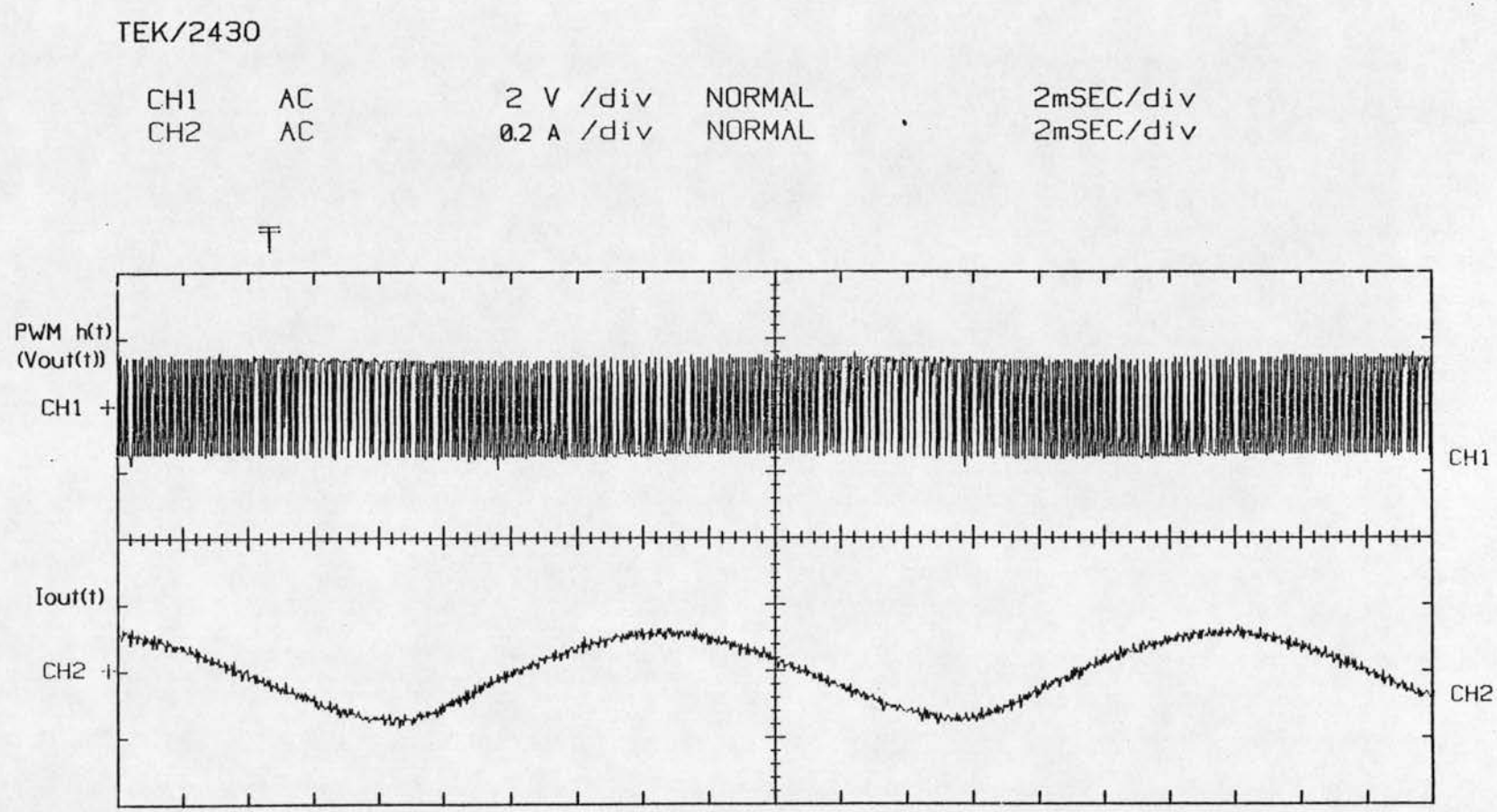


**Figure 5.10 Oscilloscope Waveforms for PWM Half-Bridge Inverter**

Figure 5.9 depicts the modulating function for phase A with the required dc offset. The corresponding PWM switching function at 180 kHz is also illustrated. The output voltage across $R$-$L$ is of the same form as the switching function, which is again shown in Figure 5.10 and can be viewed as a sine wave if appropriate filters are used. The output current is filtered (to isolate $f_{out}$ from unwanted frequency components) through $L$, and gives a better picture of the output waveform. It is a sine wave at 60 Hz, converted from a dc voltage source. The ripple observed in the waveform denotes the switching ripple (rise and fall times of current through $L$) during switching. The results are consistent with theory.

### 5.5 Two-Phase - Single-Phase Universal and Slow Switching Frequency Changers

All ac-ac converters require that the switching functions contain a Fourier component at frequency $f_{sw}=f_{in}\pm f_{out}$. The most straightforward way to accomplish this is to set $f_{sw}$ to either the sum or difference of the input and intended output frequencies. Thus, a conversion of 60 Hz to 40 Hz would result if a switching frequency of either 20 Hz or 100 Hz were applied. This is equivalent to a linear phase modulation.

The choice of adding the input and the output frequencies is given the name "universal frequency changer" (UFC) since it works for any choice of $f_{in}$ or $f_{out}$. The choice of the difference between $f_{in}$ and $f_{out}$ gives rise to a "slow switching frequency changer" (SSFC), which has at least the constraint $f_{in}\neq f_{out}$. A simple two-phase ac to single-phase ac midpoint converter is shown in Figure 5.11. The two-phase input is represented by two voltage sources, $V_A$ and $V_B$, 180° out of phase with respect to each other. The switching function (sum or difference of $f_{in}$ and $f_{out}$) is applied to the bilateral switches. The output voltage is observed across $R$, $f_{in}$ is given at 60 Hz, and $f_{out}$ is requested at 40 Hz through the software. The microcontroller outputs the required switching function for an UFC or SSFC.

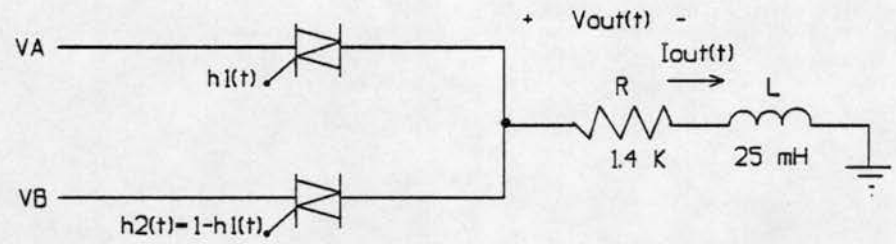


**Figure 5.11 Two-Phase ac to Single-Phase ac Midpoint Converter**

The expected output voltage waveforms for an UFC and SSFC are shown in Figures 5.12 and 5.13, respectively. The corresponding oscilloscope outputs are depicted in Figures 5.14 and 5.15, respectively.

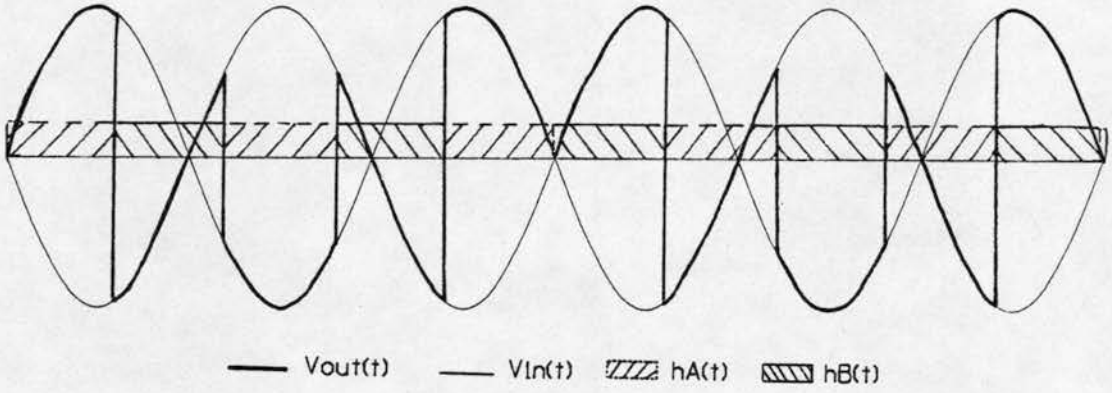


**Figure 5.12 Typical Waveforms for 60 Hz - 40 Hz UFC**

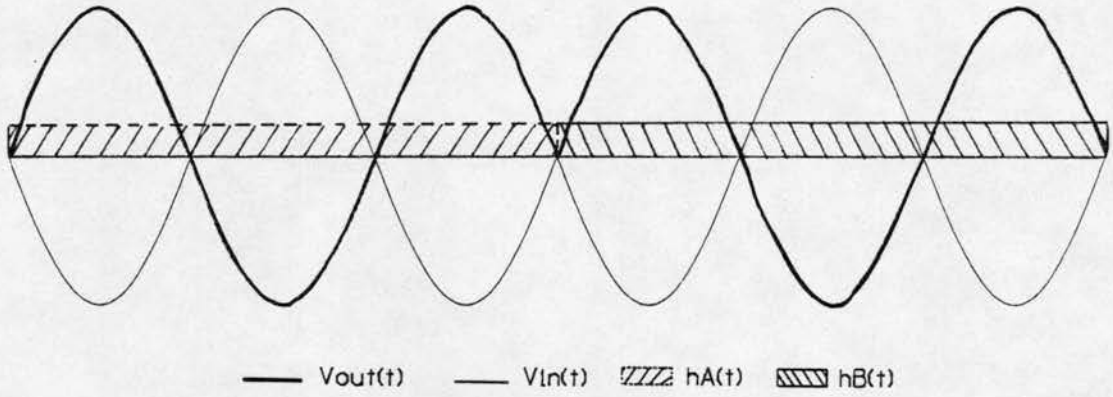


**Figure 5.13 Typical Waveforms for 60 Hz - 40 Hz SSFC**

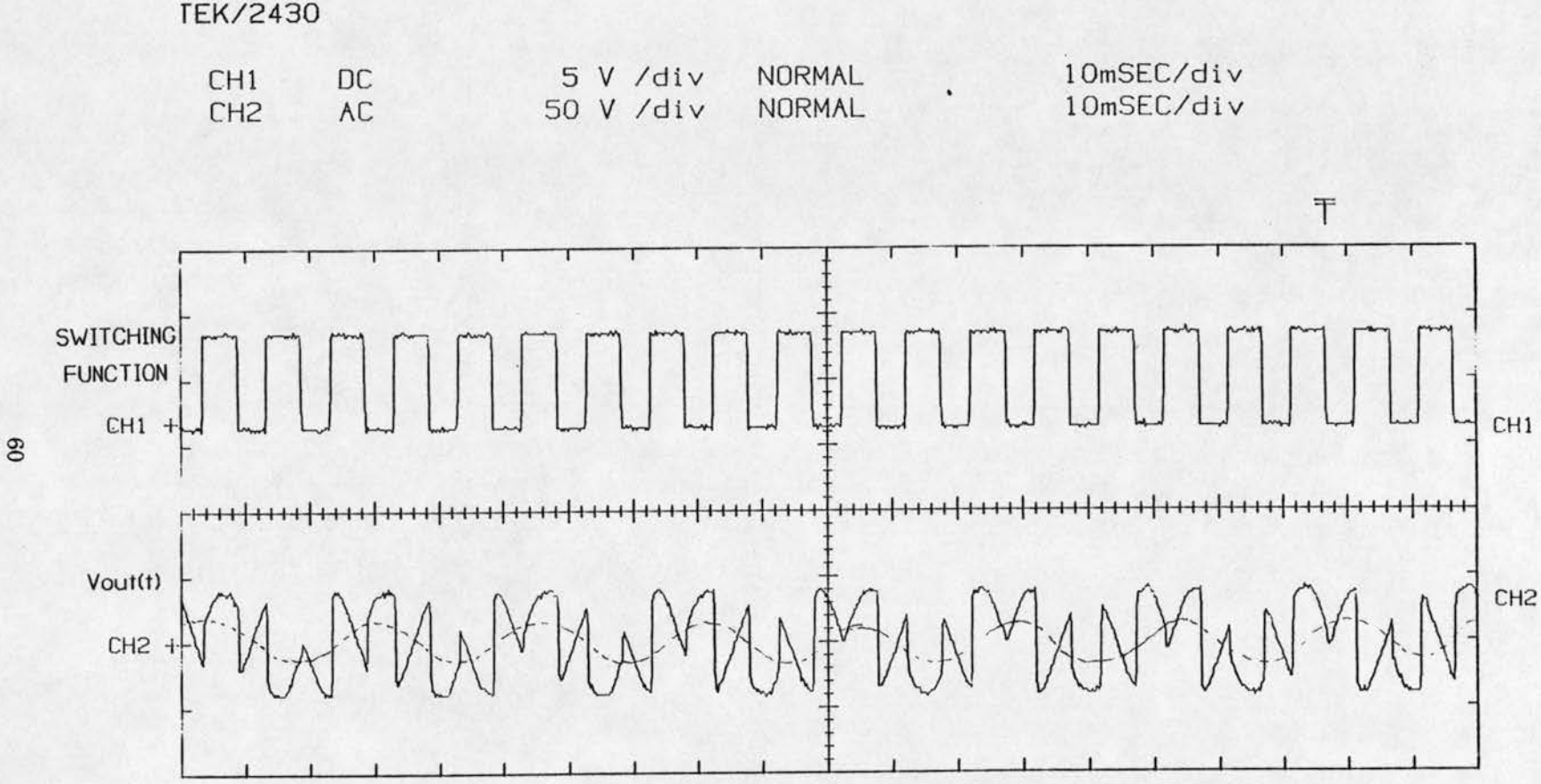


**Figure 5.14 Oscilloscope Waveforms for 60 Hz - 40 Hz UFC**

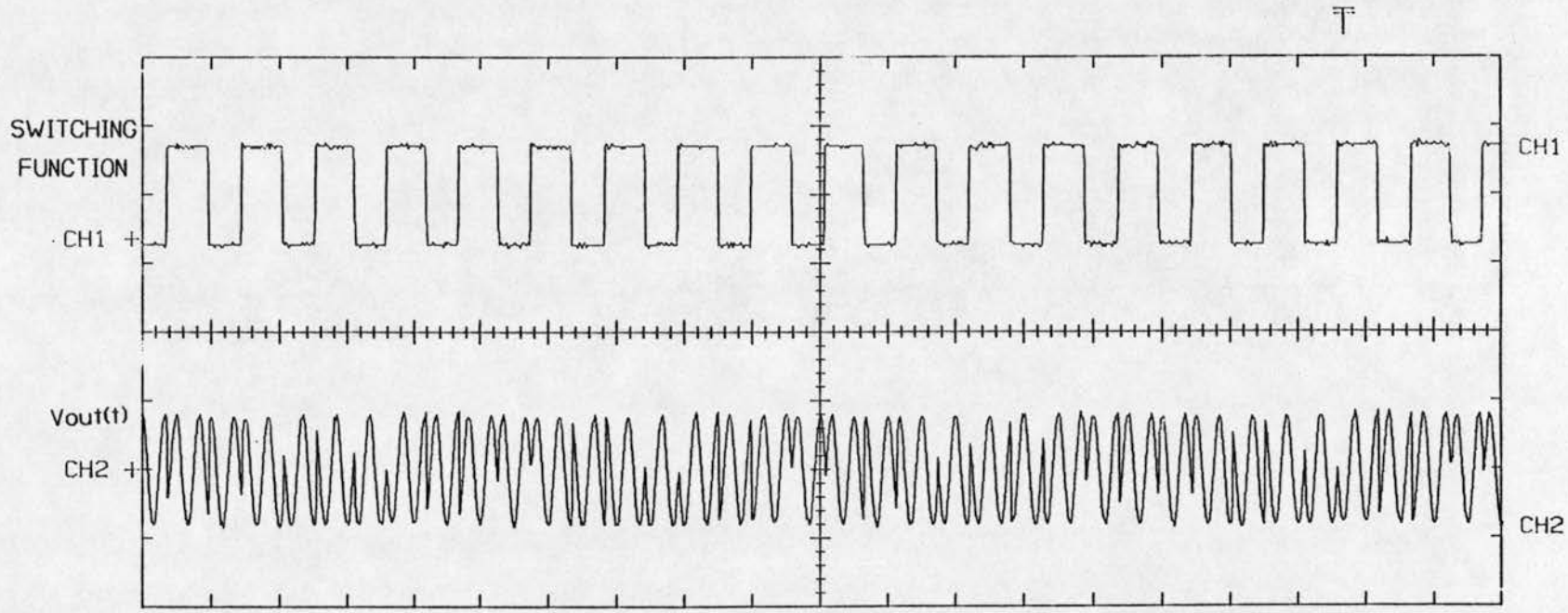


**Figure 5.15 Oscilloscope Waveforms for 60 Hz - 40 Hz SSFC**

The switching frequency is (60+40) Hz, that is, 100 Hz for an UFC, and (60-40) Hz, that is, 20 Hz for a SSFC. The output voltages contain a Fourier component for the frequency at 40 Hz. The results are consistent with theory.

### 5.6 Conclusions

The results illustrated above demonstrate the efficacy of the test bed as a generic controller for switching power converters. Other than controlling the basic power conversions, the test bed has wide scope for a variety of other applications. It can be used to test different concepts in power converters and motor control techniques. In other words, the test bed is a generalized "real" experimental system. The flexibility to test out any system topology in actual practice, as compared to simulation, makes the system a very efficient research tool. It is able to implement almost any control method for the analysis of switching power converters.

The uniqueness of the system arises from its capability to act as a three-phase function generator (square, triangle and sine waves) with all parameters being controlled through software. The system can thus output any switching function or modulating function of desired frequency. Switching frequencies up to 350 kHz are made possible through an isolated gate drive circuit. The isolation helps in accessing any circuit topology quickly. High-power bilateral switches make practical power conversions possible. The intelligent control action of the microprocessor helps in performing detailed studies of waveforms and converter dynamics in real time. Being a "real" experimental system, most of the problems encountered with simulation approaches are not present. Efficient monitoring of the states of switches is easily possible. The transient characteristics of real switches can be studied directly.

Some experimental results obtained with this system have been illustrated earlier in this chapter. They are consistent with those theoretically expected. Indeed, the efficacy of the system as a fast and an accurate interactive design tool is well-demonstrated.

# APPENDIX A

# CIRCUIT DESIGN AND OPERATION

In this Appendix, the actual circuit design and operation of each stage covered in Chapter 4 are described in detail.

## A.1 The Digital Circuit

The 8052AH-BASIC has an eight-bit data bus and a sixteen-bit address bus. The lower eight bits of the address are multiplexed with the data. This requires the lower eight bits to be latched when communicating with the memory. The address/data bus is on port 0 ($P_0$), the higher-order address bits are on port 2 ($P_2$), and the I/O port is port 1 ($P_1$). A 10 MHz crystal and a reset circuit are attached separately. A standard power supply (+5 V, 1 A) is used for both the digital and the analog circuits. A three-state, eight-bit data latch, SN74LS373, is used for latching the data and the reference signals. The circuit diagram is shown in Figure A.1.

Since the microcontroller memory is filled up with the BASIC interpreter, external memory must be attached to store the software. It is more convenient to store the required software each time a power conversion is requested, rather than to store all software in an external EPROM. This not only reduces the memory requirement, but also makes editing the software more convenient; there is no need for saving the edited version in an EPROM every time. One possible way to achieve this is to attach external RAM to the microcontroller. The required software is initially stored in a PC. The software is written with the help of a commercial BASIC interpreter and stored in a text form readable by other software packages. A serial communications routine transfers the required software, line

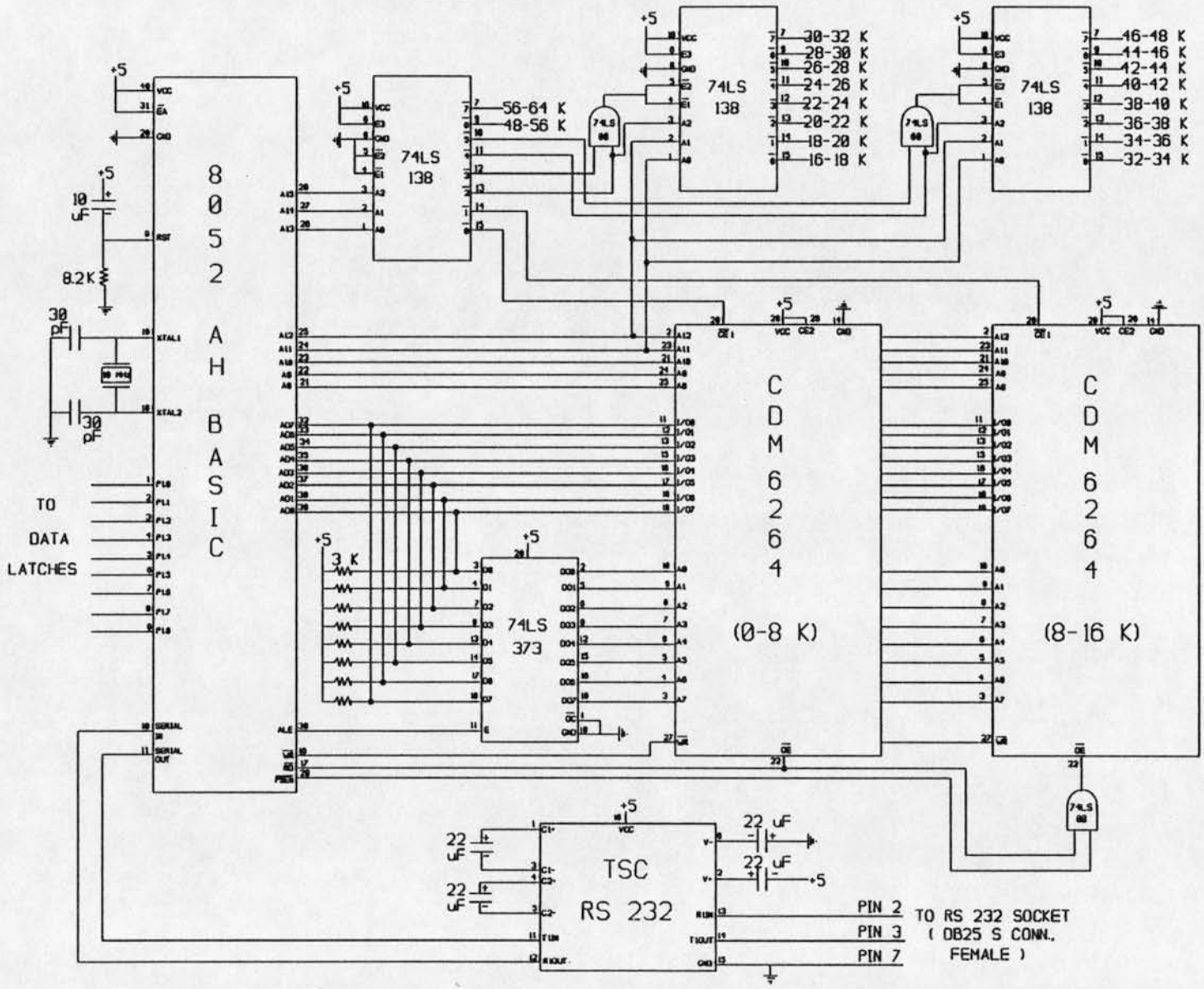


**Figure A.1 Digital Circuit Pinout Diagram**

by line, through a standard RS 232 interface, to the microcontroller. The microcontroller then stores it in the appropriate memory location in the RAM. The RAM consists of 16 K bytes (two 8 K byte SRAMS, CDM6264E). Provision has been made to increase the size of the memory in the future, if necessary.

Assembly language files are created on the PC with an editor. These files are converted to machine language, through the MCS-51 assembler, also on the PC. These files are then accessed by the same serial communications routine and are transferred line by line to the microcontroller. Assembly language files are stored only in the upper 8 K bytes of RAM, since that part of the memory is configured to emulate a ROM, and the 8052AH-BASIC permits assembly language routines to be called only from ROM. The addresses of the locations should be given appropriately, such that they do not overlap previously stored BASIC or assembly language files.

The decoder circuit consists of three 3-to-8 decoder chips, SN74LS138, in cascade. They are configured so that a sufficient number of enable signals are available for different data latches and memories. The top three address lines from port 2 ($A_{13}$-$A_{15}$) serve as inputs to the first decoder. This outputs 8 enable signals, each separated by 8 K, totalling 0-64 K bytes. The lower two output enable signals (0-8 K and 8-16 K) are used to enable the respective RAMs. The next four enable signals are then passed through two more decoders to give sixteen enable signals in the range of 16-48 K, each separated by 2 K. These are used to enable different data latches and the feedback circuit. The remaining upper two 8K enable signals are available for future expansion. Table A.1 shows the available enable signals, the range of the address locations that can activate them, and the enabled devices.

Port 1 of the microcontroller is connected to various data latches for outputting and storing the reference signals. The feedback is connected to port 0 and is read as if the

microprocessor is accessing a memory location. This makes the feedback detection and control comparatively slow. The required speed criterion could be achieved by using the interrupt facilities available on the 8052.

**Table A.1 Enable Signals and Their Functions**

| Number | Bytes | Device | Function |
|---|---|---|---|
| 1 | 0-8 K | Memory | Lower 8 K RAM |
| 2 | 8-16 K | Memory | Upper 8 K RAM |
| 3 | 16-18 K | Data Latch | dc-dc (Amplitude) |
| 4 | 18-20 K | Data Latch | dc-ac (Sine Frequency) |
| 5 | 20-22 K | Data Latch | dc-ac (Triangle Ampl.) |
| 6 | 22-24 K | Data Latch | dc-ac (Sine Amplitude) |
| 7 | 24-26 K | Data Latch | ac-dc (Phase Shift) |
| 8 | 26-28 K | Available | |
| 9 | 28-30 K | Available | |
| 10 | 30-32 K | Available | |
| 11 | 32-34 K | Data Latch | Feedback |
| 12 | 34-36 K | Available | |
| 13 | 36-38 K | Data Latch | Available |
| 14 | 38-40 K | Data Latch | Status Monitor |
| 15 | 40-42 K | Available | |
| 16 | 42-44 K | Available | |
| 17 | 44-46 K | Available | |
| 18 | 46-48 K | ADC | Error Value |
| 19 | 48-56 K | Available | |
| 20 | 56-64 K | Available | |

## A.2 The Analog Circuit

The analog circuit description covers the four power conversions: dc-dc, ac-dc, dc-ac, and ac-ac.

### A.2.1 The dc-dc conversion

A detailed circuit to produce the dc modulating function is depicted in Figure A.2. The microcontroller is made to specify a digital value for reference, through software. This value can range from 0 to 255 to vary the output analog signals from 0 onwards. But since the analog voltage range needed is +1 V to +3 V, the range of digital values is restricted. Once the digital value is specified, the microcontroller enables the data latch, SN74LS373, through the appropriate address (16-18 K, e.g., 17000). Then it outputs the digital value through port 1 which is connected to the data latch. This loads the data in the latch. Then the latch is disabled (by enabling any unused memory location), thus storing the data.

The output control of the latch is always enabled, hence the stored data is available for immediate conversion to an analog signal. A multiplying digital-to-analog converter, DAC 0808, is used here. Given a reference voltage, it multiplies this reference by the input data and outputs this scaled value of the reference. Thus, the digital input serves as a scaling factor for the reference voltage.

In the given circuit, $V_{REF}$ (+5 V) is the reference voltage at pin 14. Resistor $R_1$ is such that the reference current into pin 14 has to be less than 5 mA. Hence $R_1 > 1$ kΩ. The output at pin 4 is in the form of a current source, hence a current-to-voltage converter is needed. A high-speed operational amplifier, LF 356, is used for the purpose. The output voltage *VO* is given by the following equation:

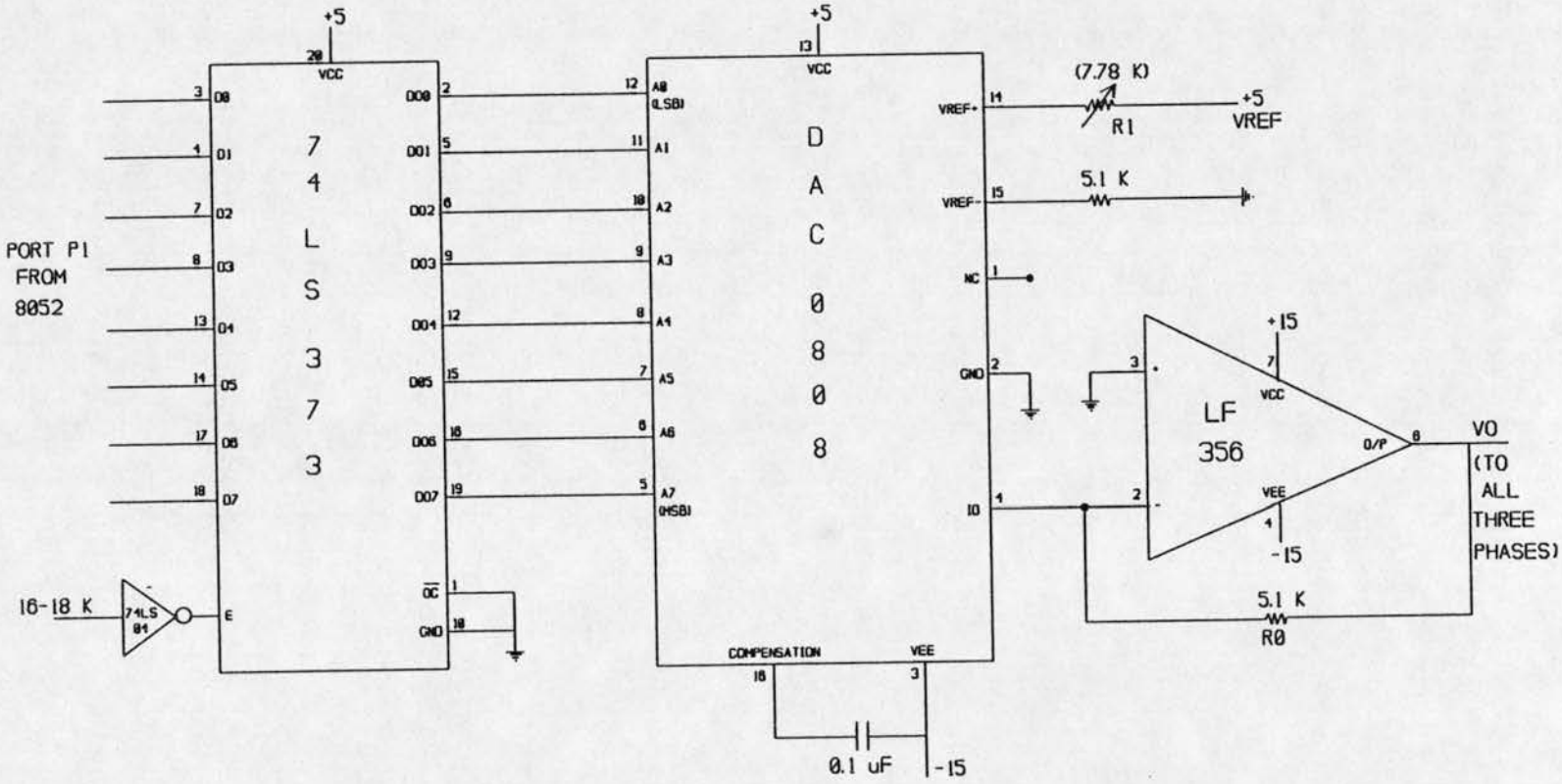


**Figure A.2 Generation of dc Modulating Function**

$$VO = -V_{REF}\frac{R_0}{R_1}\left[\frac{A_7}{2}+\frac{A_6}{4}+\frac{A_5}{8}+\frac{A_4}{16}+\frac{A_3}{32}+\frac{A_2}{64}+\frac{A_1}{128}+\frac{A_0}{256}\right]$$ ; where $A_N$ = 1 if high ; $N$ = 0 to 7
= 0 if low

To obtain about +3 V at the output, if $R_0$ = 5.1 kΩ and $V_{REF}$ = +5 V, $R_1$ has to be about 7.8 kΩ, with all the inputs high (digital value of 255). Resistor $R_1$ is a 10 kΩ potentiometer and can be trimmed accordingly for the purpose. The other external components in the circuit are in accordance with the typical values specified in the data sheets.

Voltage *VO* serves as the dc modulating function simultaneously for all three phases. It is fed as an input to the SG 3526 (switching function generator). External control for the duty cycle is also available through a ten-turn dial potentiometer on the front panel. This is a simple voltage divider circuit that varies the level of the dc modulating function between the required limits.

For multiquadrant dc-dc conversion, an external switch on the bilateral switch box connects the same switching function (phase A) to two different switches (phases A and B), each having its own complement. Thus, four switches with complementary switching functions are available.

### A.2.2 The ac-dc conversion

A detailed circuit to produce a phase-delayed, single- or three-phase switching function is depicted in Figure A.3. The data latch and the digital-to-analog converter are common to all three phases. The operation is similar to that described in Section A.2.1 (enabling address for phase delay latch is 24-26 K, e.g., 25000). To vary *VO* from 0 to about +15 V, $R_0$ is chosen as about 6 kΩ, with $R_1$ at 2.2 kΩ. Resistor $R_0$ is actually a 10 kΩ potentiometer and can be trimmed to the desired value. The analog signal *VO* is fed as a

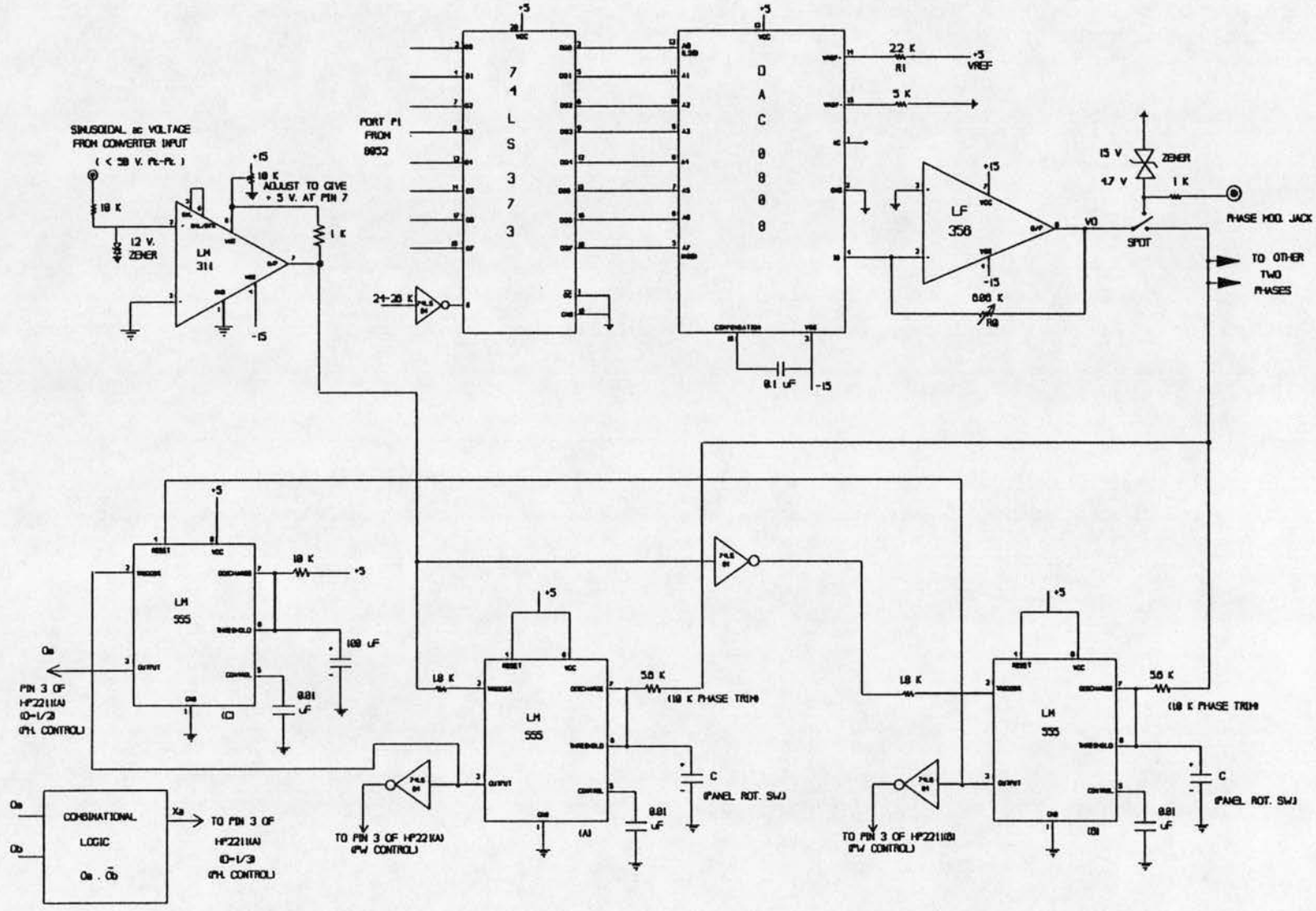


**Figure A.3 Generation of Phase-Delayed Switching Functions**

reference value to different timers for obtaining the phase delay in all three phases. The phase delay is varied by varying the level of this signal. This can also serve as a useful tool for phase modulation in ac-ac conversion; hence an SPDT switch on the side panel provides the choice of whether the microcontroller specifies the reference, or whether an externally varying voltage (for example, a triangle wave) modulates the phase of the switching function. Zener diode protection is provided to limit the external signal to 15 V. The timer circuit described next is separate for each phase.

### A.2.2.1 Timer circuit detail

In this particular application, the timer is an LM 555, configured as a one-shot. The sinusoidal ac input to the converter is applied to a voltage comparator, LM 311, through a panel jack. If the peak-to-peak ac voltage is much greater than about 50 V, it must be stepped down. A (12 V, 1 W) back-to-back Zener diode configuration with a series (10 kΩ, 0.25 W) resistor allows up to 50 V peak-to-peak input. For example, if the input is 50 V peak-to-peak, then assuming a 0.7 V drop in the Zener diode configuration, the voltage across the series resistor is (50-12-0.7), that is, 37.3 V. The current through the resistor is (37.3/10,000), that is, 3.73 mA. Power dissipated in the resistor is 0.139 W and that in the Zener is 44.8 mW, which is much less than 1 W.

The output of the comparator is used to trigger timer (A) directly, while timer (B) is triggered by inverting the square wave through a standard inverter, SN74LS04. The timers are triggered on the falling edge of the cycle. The reset pins of both are tied high to avoid false resetting. If pin 7 of both these timers was tied to the supply voltage through resistor $R$ (5.6 kΩ), the phase delay would be determined purely by the external $RC$ combination. To have a voltage control over the phase delay, the analog reference voltage $VO$ is connected

to pin 7 of each timer, in each phase, through a 5.6 kΩ resistor. This resistor is actually a 10 kΩ potentiometer and can be used for trimming the phase delay accurately in each cycle. The external capacitor $C$ is actually a set of capacitors available on a rotary switch on the side panel, and has to be set depending on the ac input frequency. Table A.2 gives the values of $C$ for different input frequencies.

**Table A.2 Timer Capacitor Values for Different Input Frequencies**

| Input Frequency (Hz) | Switch Position | Capacitance (μF) |
|---|---|---|
| 15 - 30 | 1 | 10.0 |
| 30 - 65 | 2 | 4.7 |
| 65 - 140 | 3 | 2.2 |
| 140 - 315 | 4 | 1.0 |
| 315 - 655 | 5 | 0.47 |

### A.2.2.2 Switching function generation detail

Having set the value of $C$, the phase delay is now purely controlled by the analog reference voltage, through software. The outputs of the timers (A) and (B) are passed through standard inverters, SN74LS04, and fed directly to the optocouplers in the gate drive circuit, as switching functions. These two inverted outputs, however, are not the required phase delayed switching functions. But they can be used for power conversion via pulse width control. They are of the form shown in Figure A.4.

As observed, the falling edge remains fixed, but the leading edge can have the required phase delay α. Simple applications could include ac regulators or light dimmers.

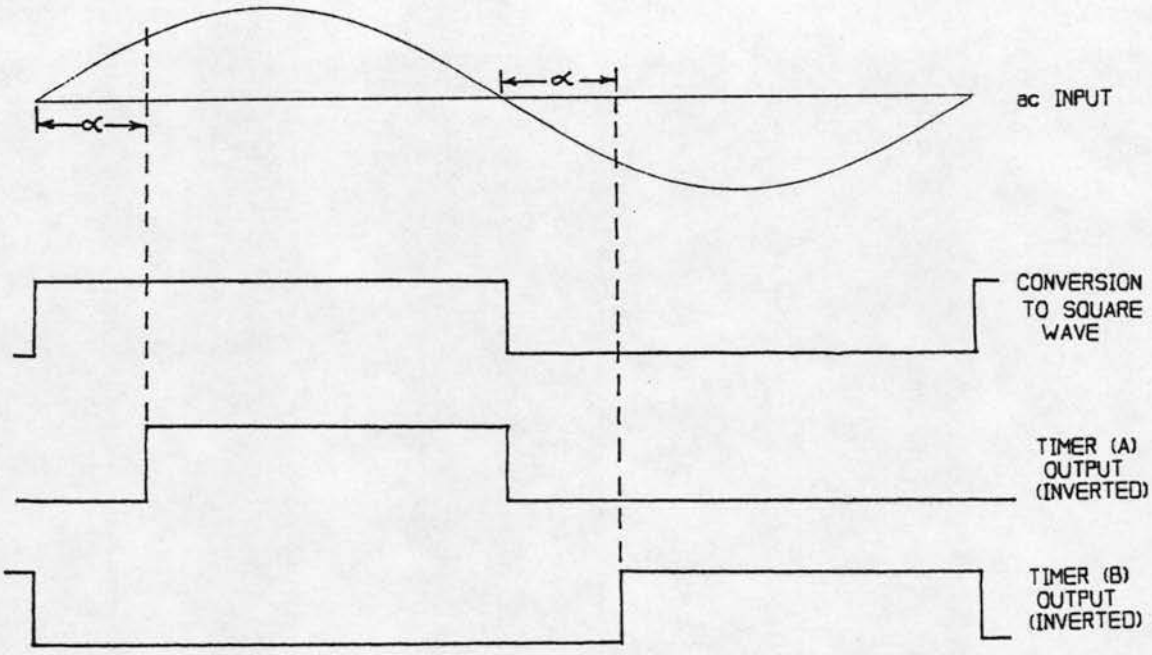


**Figure A.4 Pulse Width Control for ac-dc Conversion**

For actual phase delay in single-phase rectification, a third timer (*C*) is added to the circuit. This is best explained by the waveforms in Figure A.5.

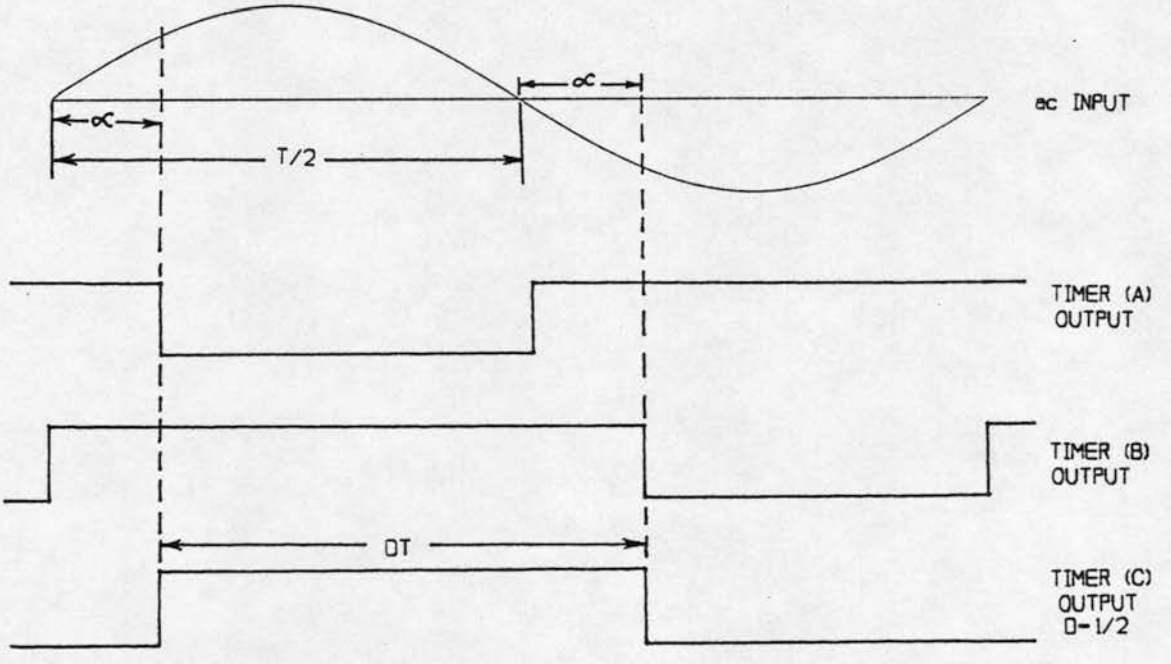


**Figure A.5 Phase-Delayed, Single-Phase Switching Function**

As observed, the falling edge output of timer (A), which has a phase delay of $\alpha$, triggers timer (C) which outputs a high instantly. This output remains high until a time $t=(1.1)RC$, or until it is reset, whichever occurs first. To use the reset function, it has to be ensured that $RC$ should be sufficiently high at very low frequencies as well. Choosing $R$ as about 10 k$\Omega$ and $C$ as about 100 $\mu$F gives a time delay of 1.1 sec which is acceptable for frequencies as low as about 1 Hz. Thus, the output of timer (C) is guaranteed to be high for all frequencies greater than 1 Hz, until it is reset. The falling edge of timer (B) which is also shifted by a phase angle $\alpha$, is used to reset timer (C).

Hence the output of timer (C), $Q_A$, is a phase-delayed, single-phase, 0 to +5 V, switching function with a duty cycle of one-half. This is fed directly to the optocoupler in the gate drive circuit. Outputs $Q_B$ and $Q_C$ for the other two phases are derived similarly. The complementary switching functions for $Q_A$, $Q_B$ and $Q_C$ are available from the gate drive circuit for the other set of switches. The three outputs of the three timers (C), $Q_A$, $Q_B$ and $Q_C$ are then processed through a combinational logic circuit to achieve a three-phase switching function having a phase delay $\alpha$. Figure A.6 explains this.

As observed, $Q_A$, $Q_B$ and $Q_C$ are displaced from each other by 120°. Each has a duty cycle of one-half. A switching function with a duty cycle of one-third and a phase delay of $\alpha$ with respect to the ac input is needed. For phase A, this switching function $X_A$ is derived by inverting $Q_B$ to $Q_B'$ through a standard inverter, SN74LS04, and performing a logical AND operation with $Q_A$, through a standard AND gate, SN74LS08; that is, $X_A=Q_A \cdot Q_B'$. This gives a duty cycle of one-third and a phase delay of $\alpha$ for the switching function of phase A. Similarly, $X_B=Q_B \cdot Q_C'$ and $X_C=Q_C \cdot Q_A'$.

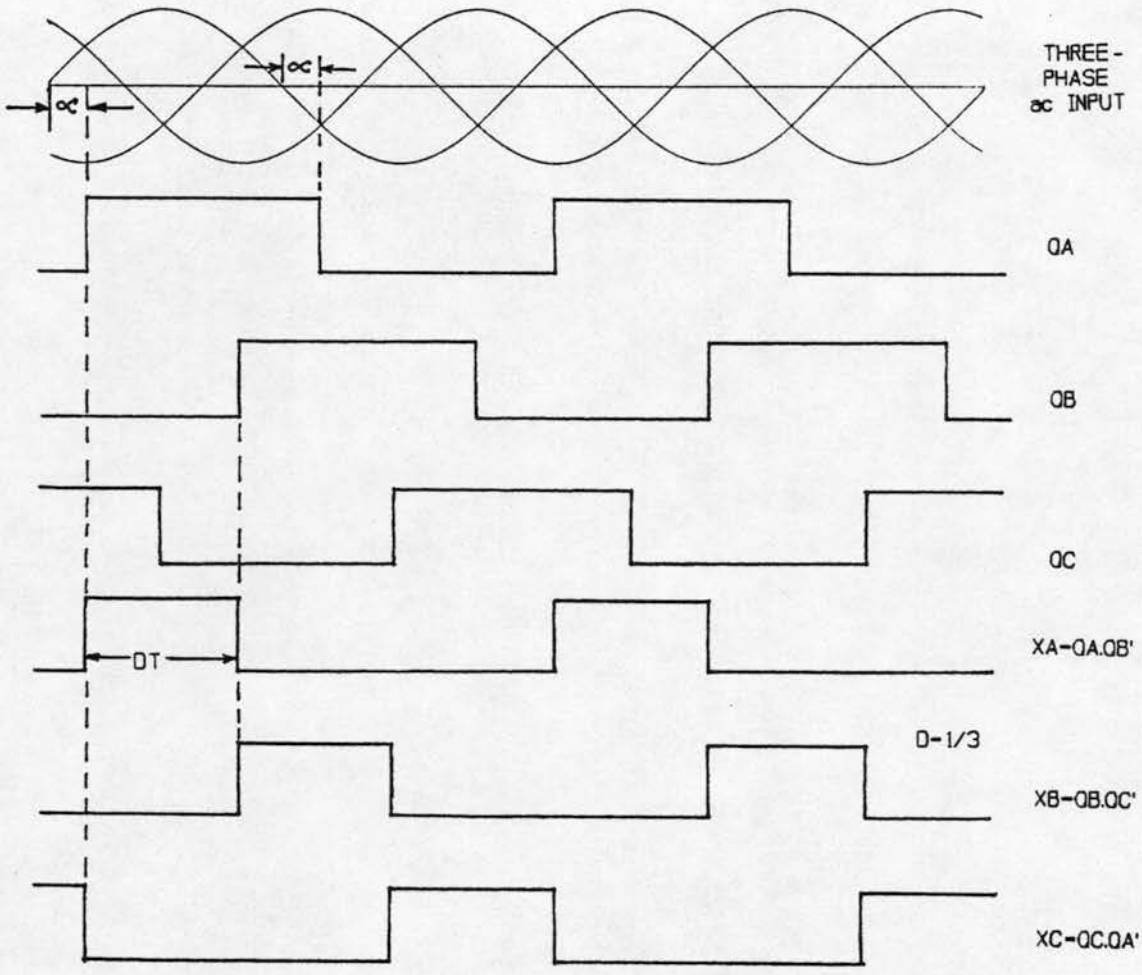


**Figure A.6 Phase-Delayed, Three-Phase Switching Function**

Thus, the required three-phase switching functions are obtained in the form of $X_A$, $X_B$ and $X_C$, which are then fed directly to the respective optocouplers in the gate drive circuit. The complementary switching functions could be made available by simply inverting them. The rise and fall times of each timer are of the order of 100 nsec, hence they do not add significantly to the phase delay $\alpha$.

Thus, a fast and precise phase-delayed switching function is available. The type desired is selected manually for each phase through a rotary switch, available on the front panel.

### A.2.3 The dc-ac conversion

A detailed circuit description to produce a three-phase sinusoidal modulating function of desired amplitude and frequency is given below.

#### A.2.3.1 Single-phase VCO detail

Figure A.7 shows the production of square and triangle waves of desired frequency through a VCO. The reference value of the frequency is loaded into the data latch and converted into an analog signal through a DAC. The operation is similar to that described in Section A.2.1. Resistor $R_1$ is selected as 2.2 kΩ. To keep *VO* in the range of 0 to about +15 V, $R_0$ has to be about three times $R_1$. Hence $R_0$ is about 6 kΩ. Resistor $R_0$ is actually a 10 kΩ potentiometer and can be trimmed as desired. The basic VCO is the LM 566 which generates square and triangle waves over a 10 to 1 frequency range. The LM 566 external timing capacitor is kept fixed at 1 μF, while the external resistor $R$ is varied through a rotary switch on the back panel, according to the frequency desired. The value of $R$ is selected as shown in Table A.3.

**Table A.3 VCO Resistor Values**

| Output Frequency (Hz) | Switch Position | Resistor $R$ (Ω) |
|---|---|---|
| 5 - 12 | 1 | 8.2 k |
| 12 - 150 | 2 | 6.55 k |
| 150 - 1450 | 3 | 140.3 |

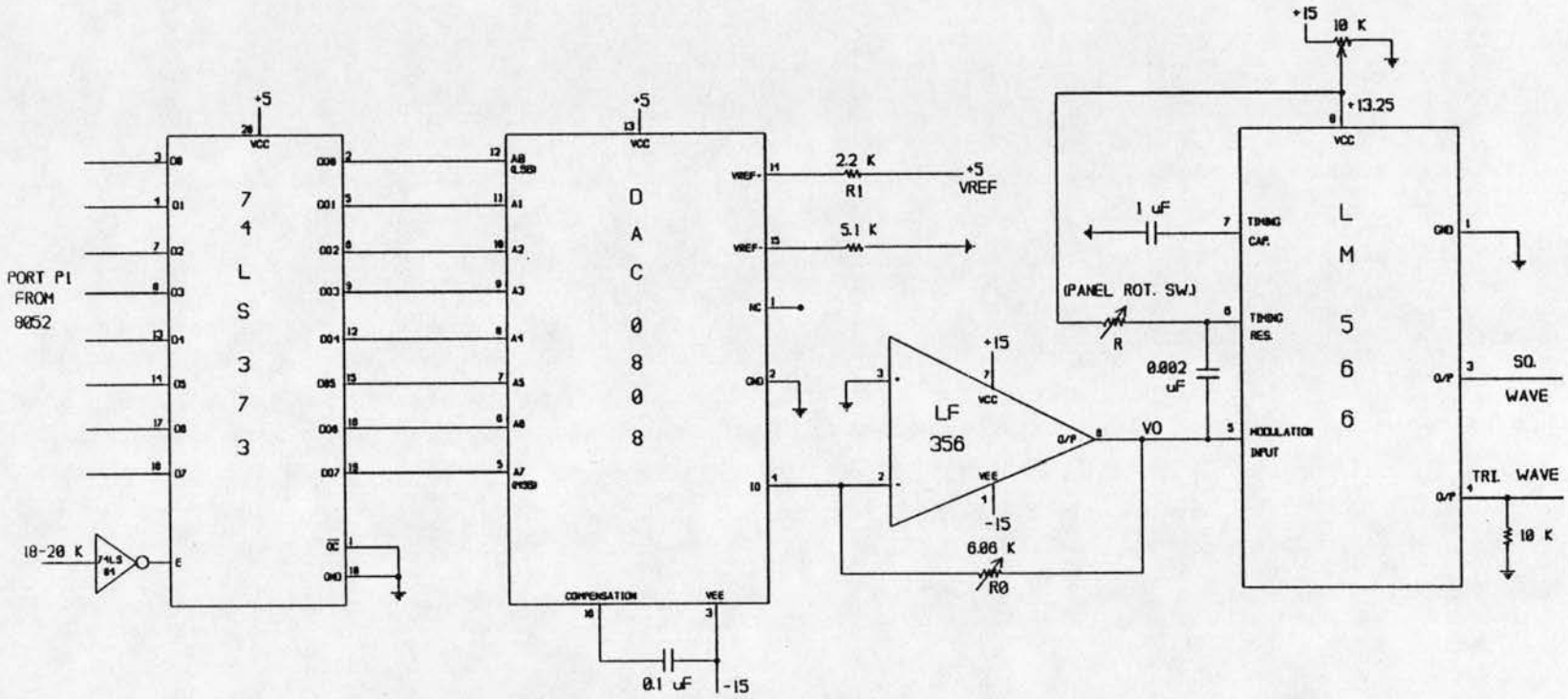


**Figure A.7 Generation of Square and Triangle Waves of Desired Frequency**

Thus, frequencies of up to about 1.4 kHz can be produced. Further ranges of frequencies are possible if either $R$ or $C$ are changed accordingly. A load resistance of about 10 kΩ is necessary at the triangle wave output (pin 4). The triangle wave has a slight dc offset. Load resistance is not necessary at the square-wave output (pin 3). The square wave has a significant dc offset of about +5 V.

### A.2.3.2 Three-phase square wave detail

Figure A.9 shows how to produce three-phase square waves with adjustable phase displacement. The basic principle used in this circuit is shown in Figure A.8. A triangle wave and a square wave with zero relative phase displacement and equal frequency are compared. The gain of the square wave can be varied from zero to the peaks of the triangle wave, centered around the midpoint of the triangle wave. The comparator output is also a square wave with a phase displacement $\phi$ from the original square wave. The value of $\phi$ varies from 90° to 180° as the gain of the original square wave is varied from 0 to the triangle wave peak. To achieve a phase displacement other than that in the above range, the triangle wave (or the square wave) can be inverted and then compared. This will vary $\phi$ from -90° to -180°.

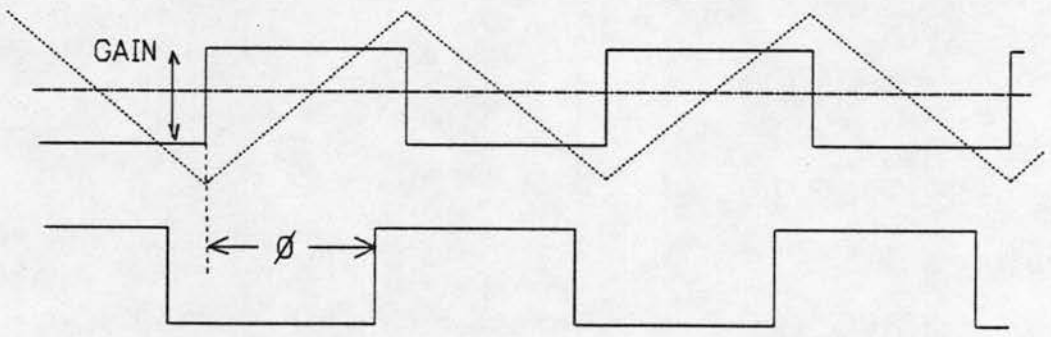


**Figure A.8 Phase Displacement Technique**

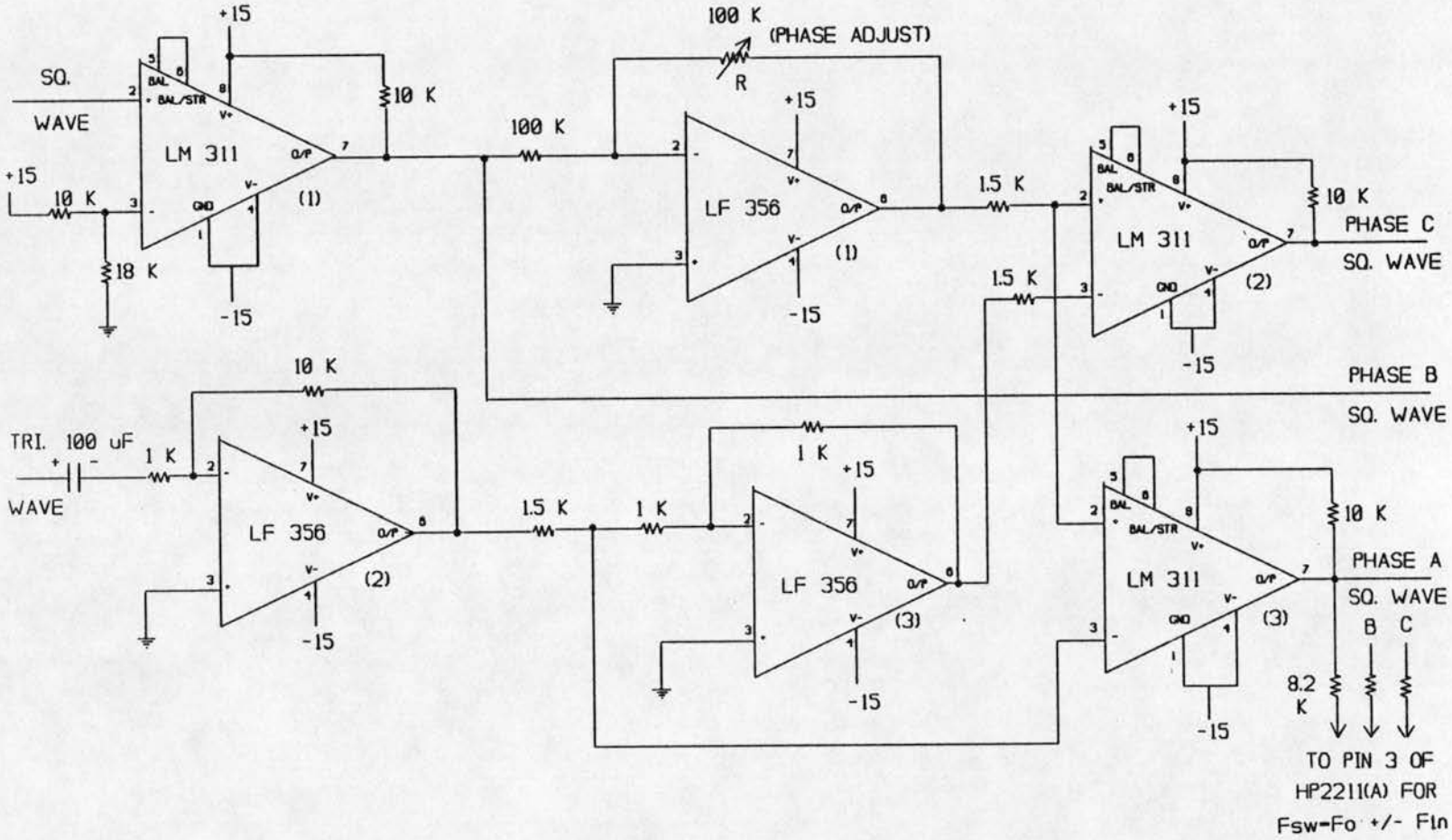


**Figure A.9 Phase Shift Circuit**

The circuit shown in Figure A.9 employs the above technique to provide two- or three-phase square waves. Initially, the dc offsets of both the triangle and the square waves are removed. The square wave is then given a variable gain through an inverting amplifier configured with an LF 356 (no. 1), by means of the feedback potentiometer $R$ (100 kΩ). Resistor $R$ is the phase adjusting potentiometer. Since the original square wave is inverted, the original triangle wave is inverted also and compared to the inverted square wave to obtain phase A (displaced from phase B by -120°), where the output is high if the square wave is greater than the triangle wave, and low otherwise. The original triangle wave is compared to the inverted square wave to obtain phase C (displaced from phase B by +120°), where the output is high if the square wave is greater than the triangle wave, and low otherwise.

The dc offset of the triangle wave is removed simply by a series capacitor. A value of about 100 μF permits operation at any frequency above 1 Hz. The triangle wave is amplified to a peak-to-peak value of about +15 to -15 V. In the process it is inverted too, since an LF 356 (no. 2) in the inverting amplifier configuration is used. This is then compared via LM 311 (no. 3) to the output of LF 356 (no. 1) to give phase A. It is also inverted once more through LF 356 (no. 3) and compared via LM 311 (no. 2) to the output of LF 356 (no. 1) to give phase C.

The phase adjustment is done via the phase adjust potentiometer $R$ and can provide a phase displacement of +90° to +180° and -90° to -180° with respect to phase B. This can produce two-phase square waves (phase displacement of 90°) or three-phase square waves (phase displacement of 120°), varying from +15 V to -15 V. For more than three phases, the phase displacement would need to be 0 to +90° and 0 to -90°. The three-phase square wave outputs are also passed directly to the optocouplers in the gate drive circuit to perform

simple dc-ac or ac-ac conversion, in which the switching frequency (a square wave) is simply the difference of the input and output frequencies (and less than 1.4 kHz in this particular case). The above circuits were common to all the three phases. The circuits described next are separate but similar for all three phases.

### A.2.3.3 Square wave integration detail

The next step is to integrate each of these square waves to triangle waves, with the amplitude being independent of frequency. This is shown in Figure A.10. Each square wave is integrated through an operational amplifier, LF 356, configured as an integrator. Capacitor $C$ is the integration capacitor and is different for different ranges of frequency. It is changed manually via a rotary switch on the back panel (the same rotary switch as used to vary $R$ on the VCO). The values of $C$ are given in Table A.4.

**Table A.4 Integrating Capacitor Values**

| Output Frequency (Hz) | Switch Position | Integrating Cap. (μF) |
|---|---|---|
| 5 - 12 | 1 | 2.2 |
| 12 - 150 | 2 | 1.0 |
| 150 - 1450 | 3 | 0.1 |

Capacitor $C_1$ is added to compensate for undesirable high-frequency poles ($R_1C_1 \approx R_2C$). The output of the integrator is passed through a series capacitor to eliminate any dc offsets. The gain is adjusted through a multiplying DAC (DAC 1020). The configuration is similar to that described in Section A.2.1 (enabling address 20-22 K, e.g., 21000).

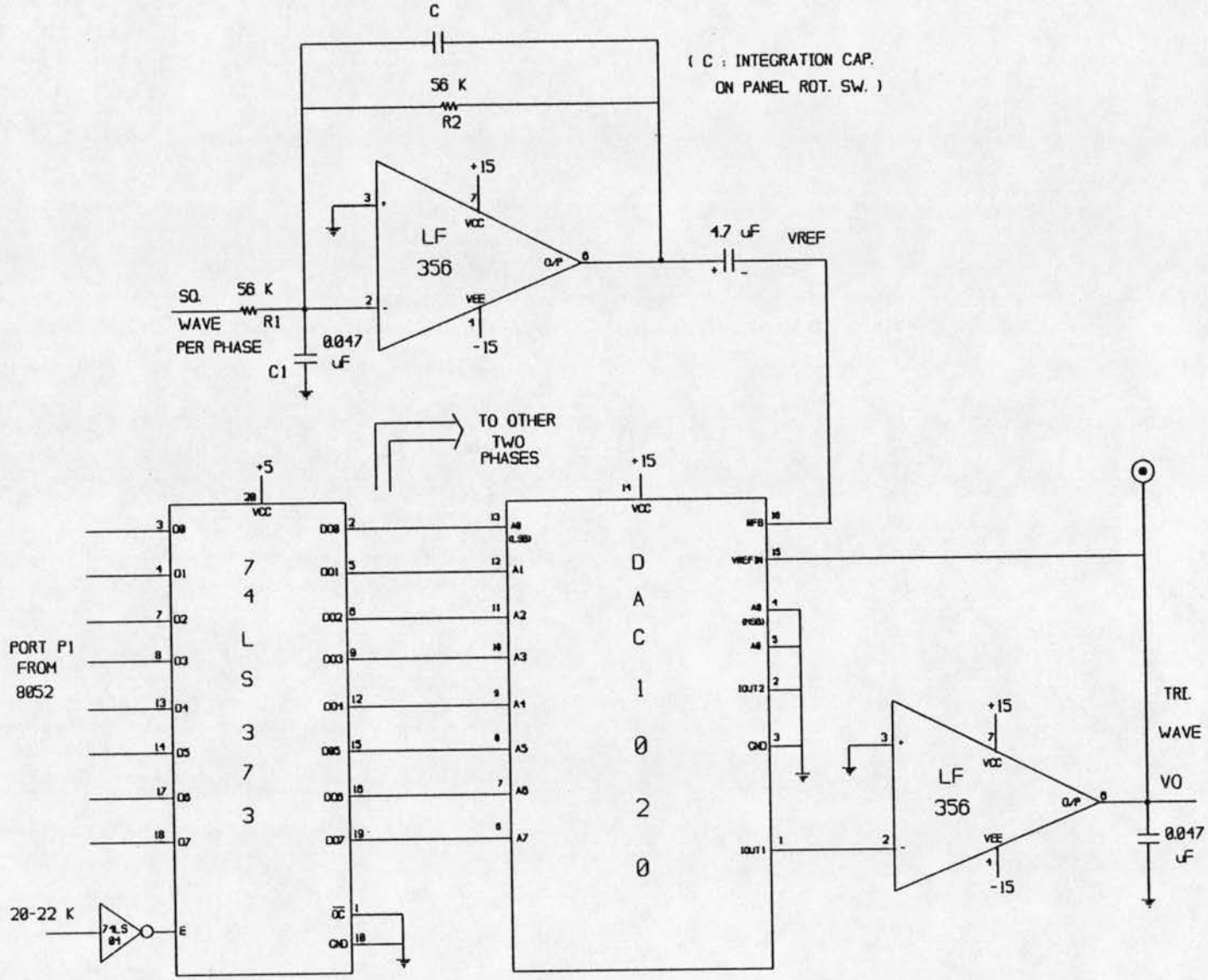


**Figure A.10 Integrator and Frequency Compensation Circuit**

The data latch is common to all three phases, with separate DACs for different phases since reference voltages are different (by a phase displacement). The output voltage *VO* of this digitally gain-controlled amplifier is given as:

$$VO = \frac{-V_{REF}}{\left[\frac{A_7}{2}+\frac{A_6}{4}+\frac{A_5}{8}+\frac{A_4}{16}+\frac{A_3}{32}+\frac{A_2}{64}+\frac{A_1}{128}+\frac{A_0}{256}\right]} \quad ; \quad \text{where } A_N = \begin{matrix} 1 & \text{if high} \\ 0 & \text{if low} \end{matrix} \quad ; \quad N = 0 \text{ to } 7$$

Thus, *VO* is always greater than or equal to $V_{REF}$. Incidentally, a gain of 0 would saturate the operational amplifier. The output *VO* (triangle wave) is always between +15 V and -15 V. Three such triangle waves displaced from each other by 120° and a zero dc offset are now available. Provision has been made to access these waves on external panel jacks for measurement.

### A.2.3.4 Diode waveshaping detail

The reason for needing a constant amplitude for the triangle waves is because diode waveshaping techniques are used to alter the triangle waves at fixed break points, such that they approximate sine waves. The break points are fixed by resistive divider circuits. The circuit is shown in Figure A.11.

The circuit consists of a chain of resistors ($R_0$ through $R_5$) connected across the entire symmetric voltage supply of +15 V, -15 V. This generates fixed break points at ±10.15 V, ±7.8 V, ±5.5 V, ±3.2 V, and ±0.88 V. The entire circuit is symmetric and approximates each quarter-cycle of the sine wave by six straight-line segments [37]. The same principle is used also in many commercial sine wave oscillators. These chips were not used here because of the phase displacement needed between different sine waves.

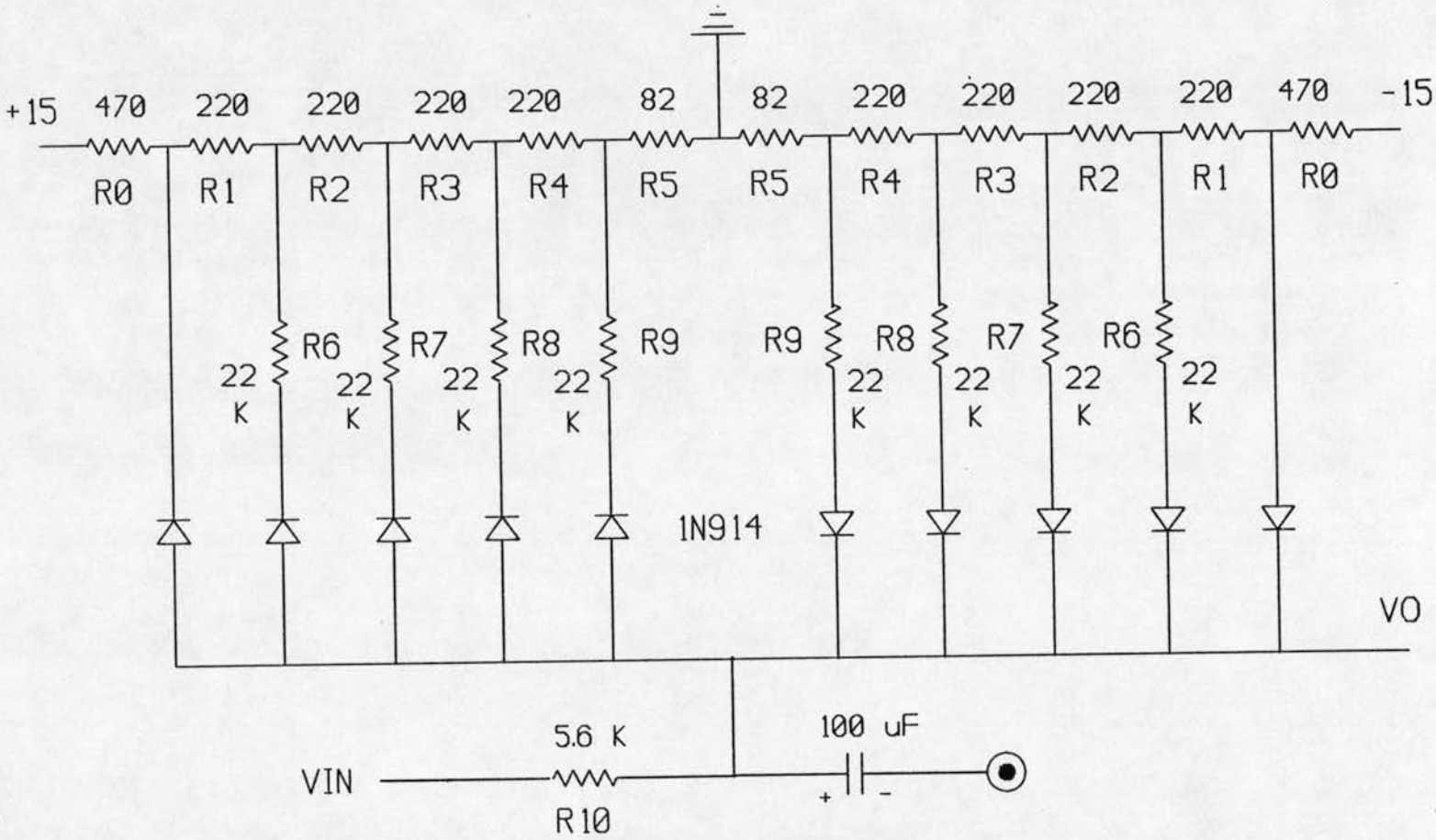


**Figure A.11 Waveshaping Circuit**

The output *VO* is an approximate sine wave between +8.3 V to -8.3 V, with a zero dc offset voltage. Three such outputs with a phase displacement of 120° from each other are available for further gain adjustment. The three outputs are also available directly to front panel jacks, through series capacitors. The series capacitor helps in rounding the edges and corners of the waveform to give a much better approximation of a sine wave. A value of 100 μF permits all frequencies above 1 Hz.

### A.2.3.5 Sine wave gain adjustment

The next step is to adjust the gain of the sine wave properly. Since this wave serves as a modulating function, it is input to the switching function generator, SG 3526. Thus, the sine wave has to have a dc offset of +2 V and a maximum amplitude of about 2 V. The required circuit is depicted in Figure A.12.

The gain adjustment is done through a latch and multiplying DAC set, as described in Section A.2.1 (enabling address 22-24 K, e.g., 23000). Since $V_{REF}$ is bipolar, a -12 V supply is connected to the DAC. Since the amplitude of the positive half-cycle of the modulating function has to be less than or equal to 1 V, a slightly higher value of about 3 V is chosen. This gives $R_0$ to be about 5.6 kΩ, with $R_1$ at 15 kΩ. Thus, $VO_1$ is a sine wave with a maximum amplitude of about 6 V peak-to-peak, at a zero dc offset voltage (ensured by a series capacitor). A value of 100 μF permits all frequencies above 1 Hz. To attain a dc offset of +2 V, an LF 356 configured as an unity gain inverting amplifier is connected in the final stage. The offset is varied by adjusting a 10 kΩ potentiometer $R_3$, connected to -15 V at pin 3 of the operational amplifier. Thus, $VO_2$ is a sine wave with a dc offset of about +2 V and a maximum amplitude of about 6 V peak-to-peak. In practice, the maximum amplitude turns out to be a little less, due to tolerance errors in resistor values.

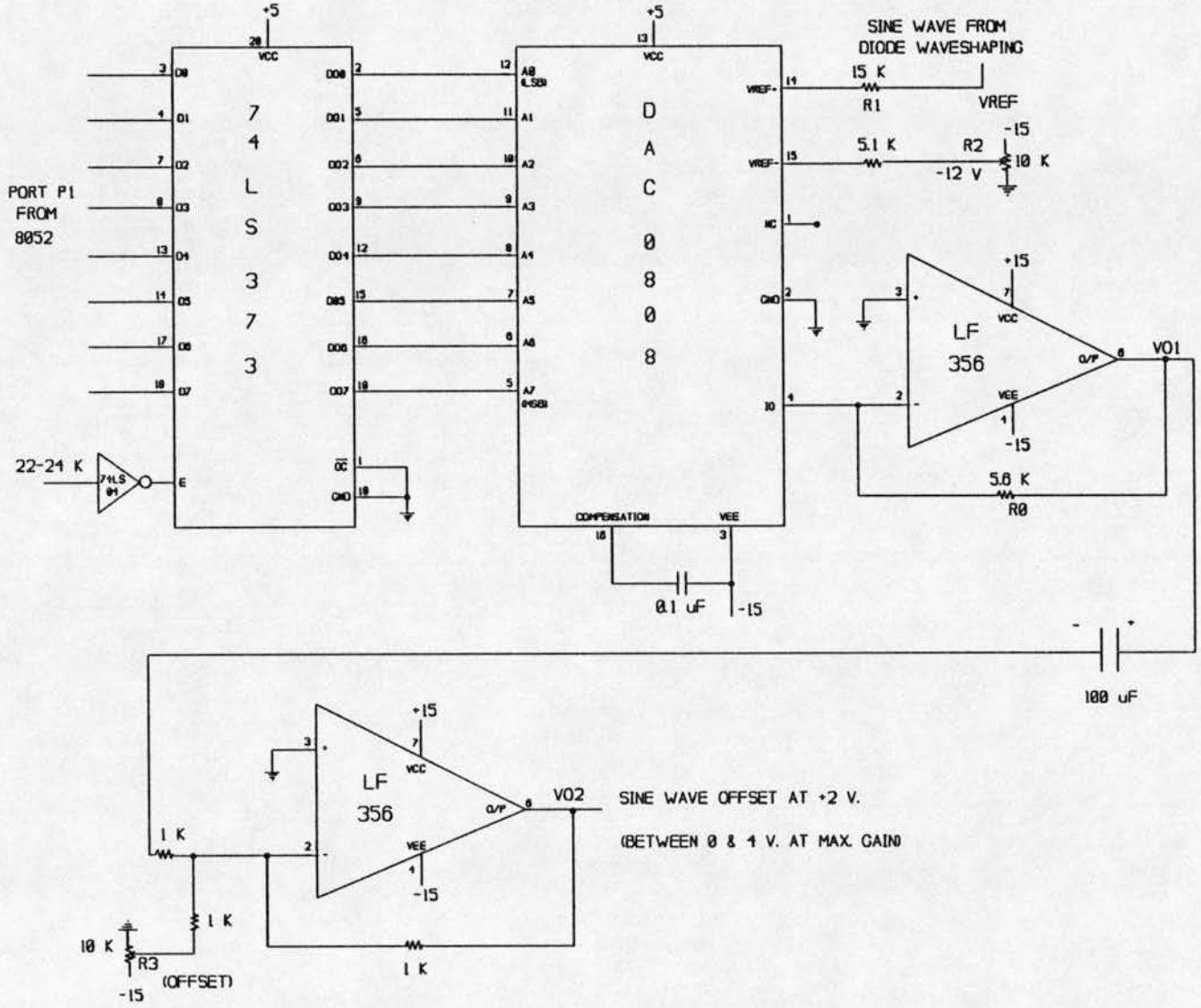


**Figure A.12 Sine Wave Gain Adjustment**

Voltage $VO_2$ is the required sinusoidal modulating function, with a variable gain and a variable frequency. Three such waveforms at desired phase displacement are available. They are input to three different switching function generators in the gate drive circuit. As mentioned earlier, the switching frequency for PWM is varied through an external knob, available on the front panel, for each phase.

### A.2.3.6 Feedback circuit

A detailed circuit is shown in Figure A.13. The microcontroller specifies a reference value (dc or ac) through a latch and a multiplying DAC set. The operation is similar to that described in Section A.2.1 (enabling address 32-34 K, e.g., 33000). The reference voltage $V_{REF}$ for the DAC 0808 is either a dc supply at +12 V or an ac sine wave. The sine wave is derived from phase A, immediately after diode waveshaping. Resistor $R_1$ is chosen as 3.9 kΩ to limit the maximum reference current. To keep the ratio $R_0/R_1$ near unity, $R_0$ is also taken as 3.9 kΩ. Resistor $R_0$ is actually a 10 kΩ potentiometer and can be trimmed as desired. Since the master operational amplifier is configured in an inverting fashion, it is preferable to have *-VO* as input instead of *+VO*. Hence *VO* is inverted through an unity gain inverting amplifier, configured with an LF 356. Thus, *-VO* is now the reference analog signal set up by the microcontroller, with which different signals from the converter output are compared through the master operational amplifier.

Four operational amplifiers are used here for four different feedback inputs : V, I, T, and one for future expansion. Each is set up in a differential mode. The four operational amplifiers are part of a single quad op-amp chip, MC 34084. Fast switching diodes, 1N 4150, are connected in anti-parallel across the input pins of each operational amplifier for protection. The output of each operational amplifier has to be close to the reference specified

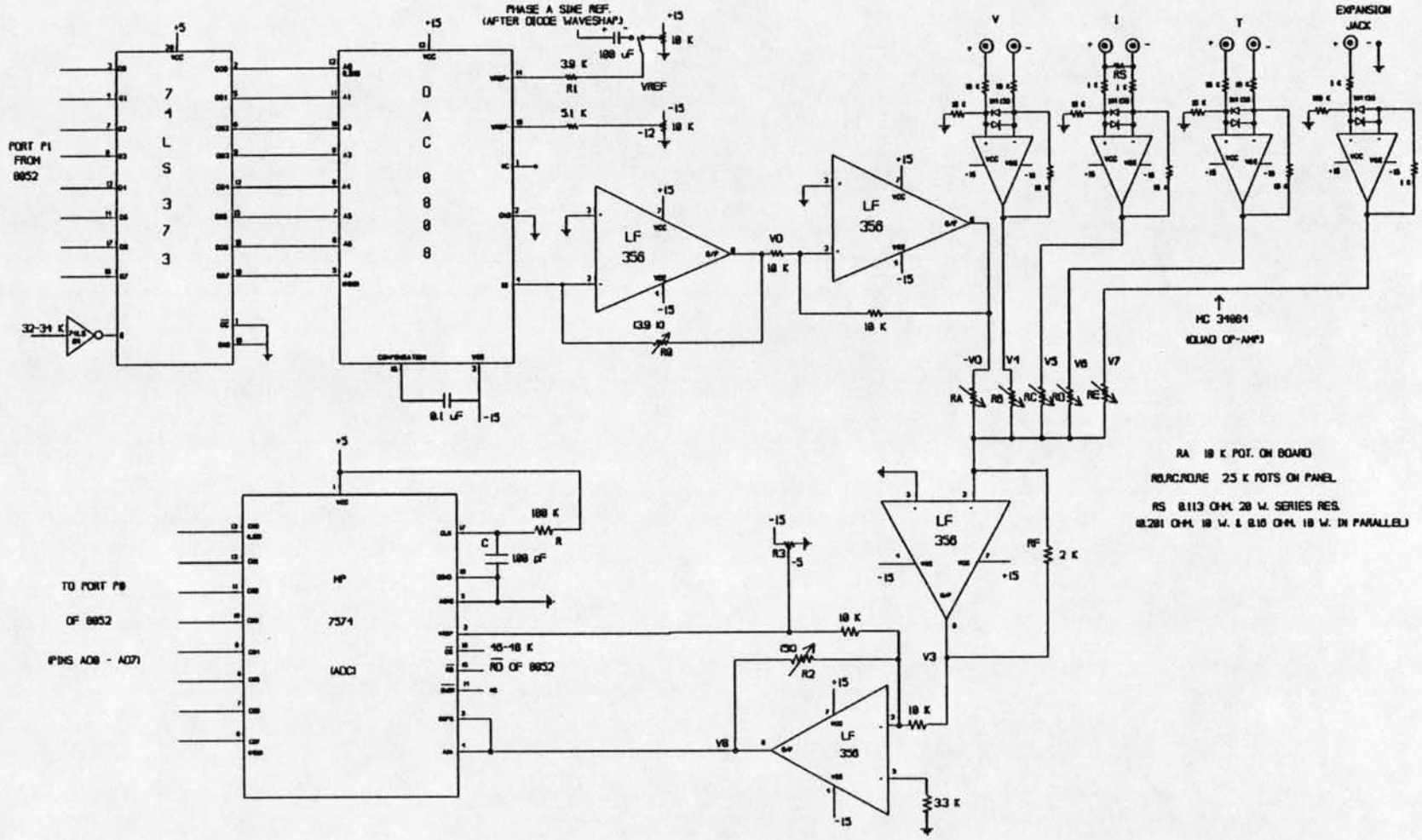


**Figure A.13 Feedback Circuit**

by the microcontroller; hence if needed, the inputs to the operational amplifiers should be stepped down first, such that the maximum possible input is 12 V. The current input is taken as the voltage across a low series resistance, $R_s$, (0.113 Ω, 20 W; configured by two 10 W resistors in parallel - 0.201 Ω and 0.160 Ω) placed in series with the output of the converter. All operational amplifiers other than that for current input are configured for unity gain. The current input operational amplifier has a gain of ten. The four inputs give rise to four feedback signals, $V_4$ through $V_7$. These are input to the master operational amplifier, LF 356, in conjunction with the reference voltage $-VO$, specified by the micrcontroller. The output of the operational amplifier is the error signal $V_3$ and is given as follows:

$$V_3 = -R_F\left(\frac{VO}{R_A} - \frac{V_4}{R_B} - \frac{V_5}{R_C} - \frac{V_6}{R_D} - \frac{V_7}{R_E}\right)$$

Resistors $R_A$ through $R_E$ are adjustable, hence, $V_3$ is of the form

$$V_3 = -K_A VO - K_B V_4 - K_C V_5 - K_D V_6 - K_E V_7$$

where $K_A$ through $K_E$ are constants.

Resistor $R_A$ is a 10 kΩ potentiometer mounted on the board; $R_B$ through $R_E$ are 2.5 kΩ potentiometers on the back panel. Resistor $R_F$ is fixed at 2 kΩ; $R_A$ is set equal to $R_F$ for most purposes.

The analog error signal, $V_3$, must be converted to an equivalent digital form so that it can be fed to the microcontroller, which in turn can process it and take the required action to modify the switching function. An analog-to-digital converter is necessary for this purpose. An eight-bit microprocessor compatible analog-to-digital converter, AD 7574, which uses the successive-approximations technique to provide a conversion time of about 15 μsec, and which can be interfaced to a microprocessor like a static RAM or ROM, is used. The

internally latched output data bits are tri-stated, allowing direct connection to the microprocessor data bus or the system I/O port. In this application, it is operated in the bipolar mode, to allow positive or negative error signals. Since reference voltage, $V_{REF}$, at pin 2 is -5 V (achieved through a voltage divider 10 kΩ potentiometer connected to the -15 V supply), the nominal analog input range is -5 V to +5 V. The analog-to-digital converter is actually fooled into believing that it is operated in an unipolar mode, that is, the +5 V to -5 V analog input is conditioned into a 0 to +5 V signal range by means of an inverting operational amplifier configured by an LF 356. The output, $V_8$, at pin 6 of the operational amplifier is given as

$$V_8 = -\frac{R_2}{10\ k\Omega}(V_3 - V_{REF}\frac{10\ k\Omega}{10\ k\Omega})$$

Voltage $V_3$ varies from -5 V to +5 V; $V_{REF}$ is -5 V. Hence if $R_2$ is set at 5 kΩ, $V_8$ can vary from 0 to +5 V. Resistor $R_2$ is actually a 10 kΩ potentiometer and can be set as desired. The resolution of the AD 7574 in the bipolar mode is (1/128)($V_{REF}$), that is, (1/128)(5 V). It has an internal asynchronous clock oscillator and needs an external resistor and capacitor as shown, which are chosen from the graphs in the data sheets. The value of the resistor may be decreased a little to decrease the conversion time, as long as the ambient temperature is within limits. The converter is connected directly to the data bus of the microcontroller, that is, to port 0.

A convert start is initiated by executing a memory WRITE instruction to the appropriate address location (46-48 K, e.g., 48000) for selecting the chip. After the conversion delay, a data READ is performed by executing a memory READ instruction to the same address location, after which it is disabled. The error is zero if the digital output is equal to 128, positive if it is greater than 128, and negative otherwise.

The circuit diagram for the "Status Monitor" is depicted in Figure A.14. The feedback signals are fed in the same way as described above. All outputs (*VO*) of the comparators are connected directly to a three-state data latch, SN74LS373. Pull-up resistors (1 kΩ) are necessary at each output. These are in the form of a stack of resistors connected directly to the input pins of the data latch. At present, only four input pins are utilized. The four most significant input pins of the latch are left open for future connections. The output pins of the latch are again directly connected to the system data bus, that is, to port 0 of the microcontroller. The data can be read by the memory READ instruction which enables the latch, once the latch has its output control activated by the appropriate address (38-40 K, e.g., 39000).

### A.3 The Switch Matrix and Gate Drive Circuit

The detailed circuit for one phase is depicted in Figure A.15. The description is divided into three parts: the switching function generator circuit, the isolated power supplies, and the bilateral switches.

The switching function generator circuit comprises the switched-mode power supply control circuit, the optocouplers, the high-current buffers, and the function-select rotary switch. The switched-mode power supply control circuit, SG 3526, operating from a single +15 V supply (pin 17), is configured to output switching frequencies from 10 kHz up to about 350 kHz. A lower range is possible by increasing the value of the capacitor (0.002 μF) $C_t$, connected to pin 10. Switching frequency is controlled by the external 100 kΩ potentiometer $R_t$ at pin 9, available on the front panel. The duty ratio can also be controlled through a 100 kΩ potentiometer at pin 1, available on the front panel. This is essentially a voltage divider circuit, attached from +5 V ($V_{REF}$, pin 18 of SG 3526, is an internal +5 V

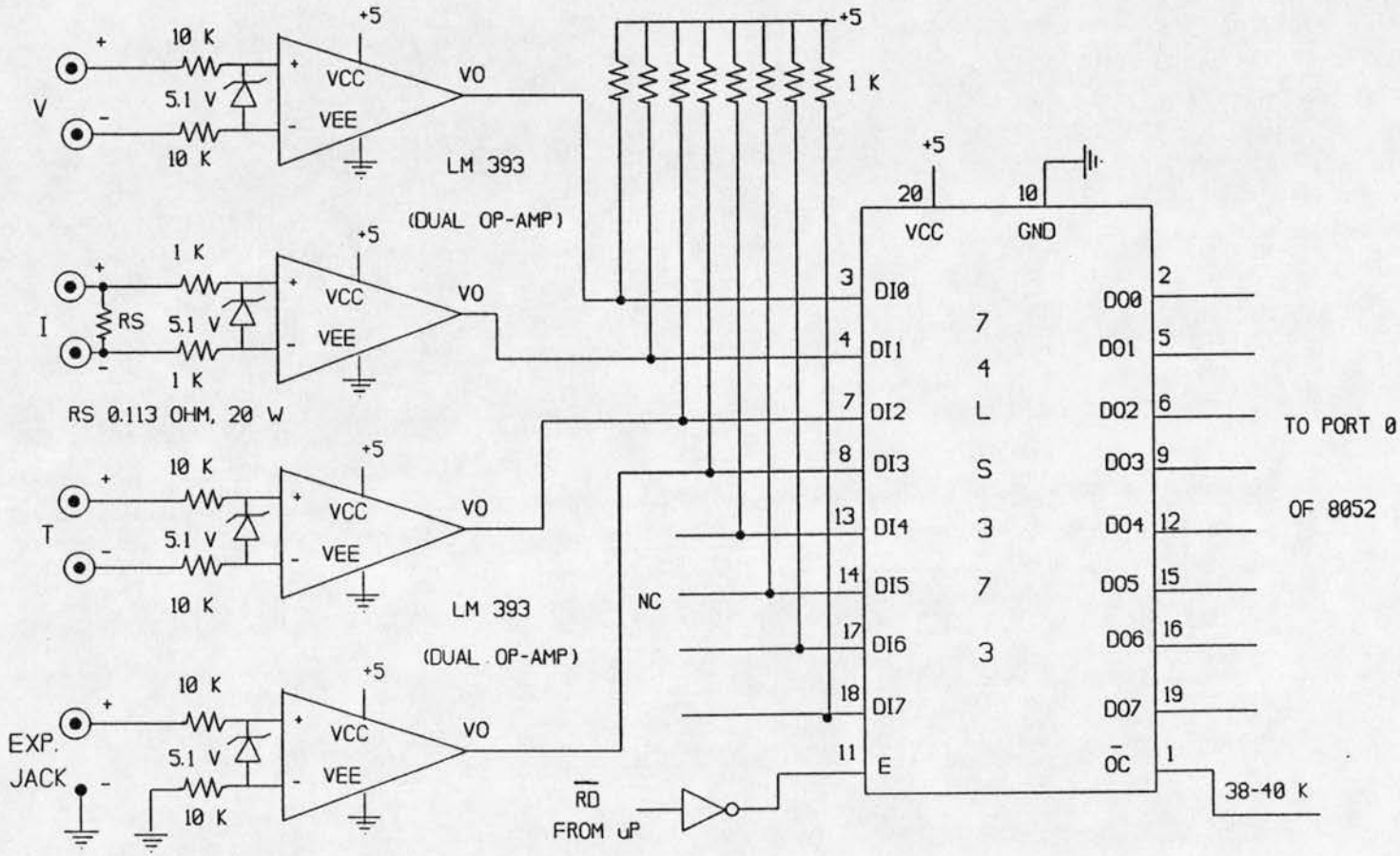


**Figure A.14 Status Monitor**

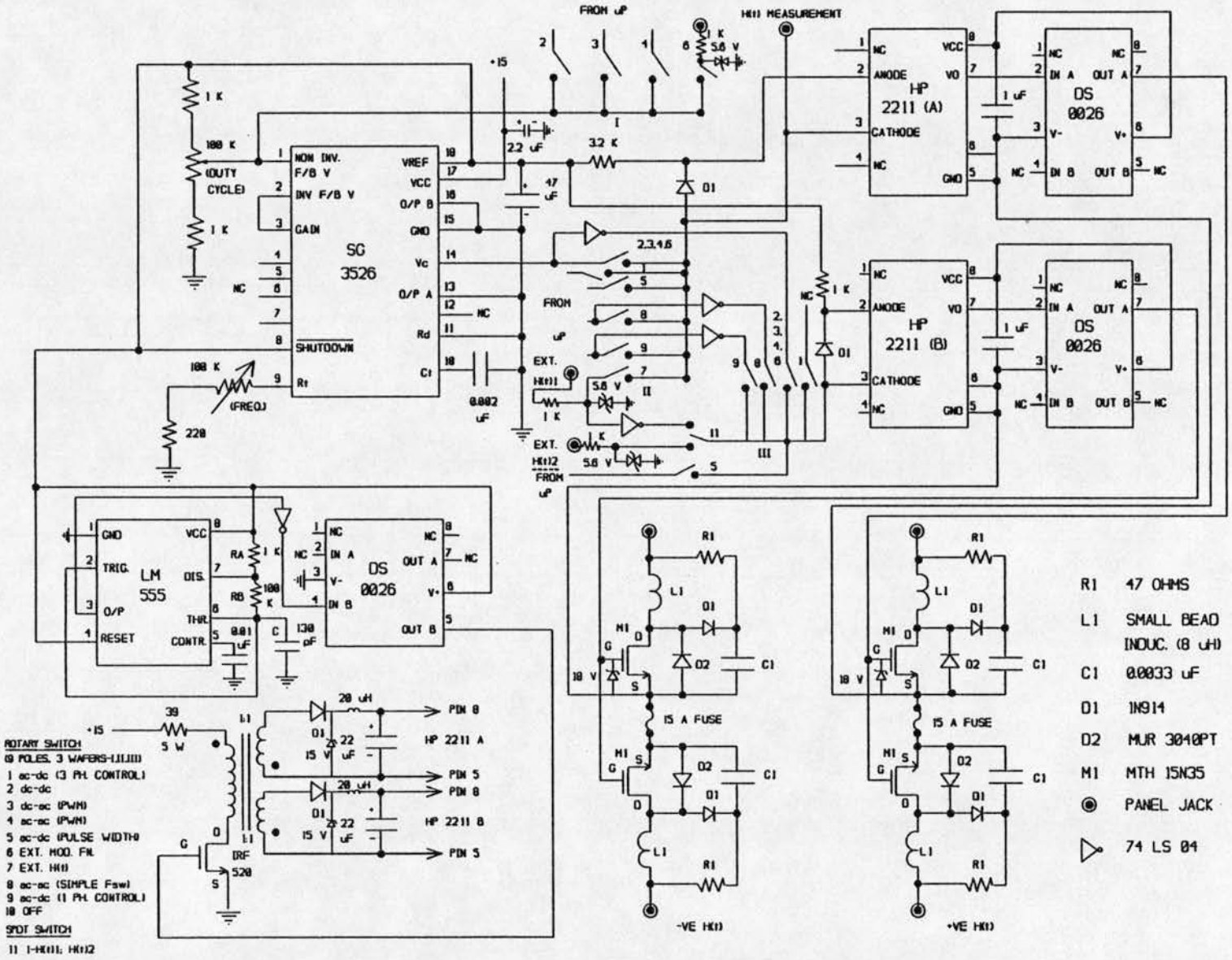


**Figure A.15 Gate Drive Circuit with Bilateral Switches**

regulator) to ground. The potentiometer varies the level of the dc voltage between +1 V and +3 V which serves as a dc modulating function. The SG 3526 has an internal ramp generator which generates a triangle wave at the switching frequency, and which varies between +1 V to +3 V peak-to-peak. The modulating function is compared to this triangle wave to output a switching function at pin 14, which is also available for measurement through a terminal jack on the external panel. The external duty cycle control can be overridden by the low output impedance modulating functions from the microcontroller or from an external source. This is achieved with the help of a function-select rotary switch (positions 2, 3, 4 and 6) for different modulating functions. A 1 kΩ series resistance and a 5.6 V back-to-back Zener diode configuration is provided for overvoltage protection at the external modulating function input jack (on the front panel) for each phase. An arrangement is provided for an external switching function input also. A similar overvoltage Zener diode protection is provided at this external jack. The limits for the external modulating or switching function inputs are 0 to +5 V. As mentioned earlier, different conversion functions are performed by manually setting the function-select rotary switch for each phase at the required position. The various positions of the function-select rotary switch are shown in Table A.5.

Positions 2, 3, 4 and 6 are for modulating functions only. Positions 1, 5, 8 and 9 are for direct switching functions, input from the microcontroller to the optocoupler. Positions 7 and 11 (SPDT switch) are for external switching function inputs from front panel jacks (having 1 kΩ series resistance and 5.6 V back-to-back Zener diode configuration for protection). Position 10 is the "off" position. The remaining hardware particulars and specific connections of the function-select rotary switch along with the corresponding diagrams are described in Appendix B.

**Table A.5 Function-Select Rotary Switch Positions**

| Position Of Rotary Switch | Function |
|---|---|
| 1 | ac-dc (Three-phase control) |
| 2 | dc-dc |
| 3 | dc-ac (Pulse width modulation) |
| 4 | ac-ac (Pulse width modulation) |
| 5 | ac-dc (Pulse width control, e.g., ac reg.) |
| 6 | External Modulating Fn. (Panel jack); (External knob control for duty cycle) |
| 7 | External Switching Fn. (Panel jack) |
| 8 | ac-ac, dc-ac ($f_{sw}=f_o \pm f_{in}$) |
| 9 | ac-dc (Single-phase control) |
| 10 | Off |

| | |
|---|---|
| SPDT switch (# 11) | External Switching Fn. $H(t)_2$ or Complement of External Sw. Fn. $H(t)_1$ |

The various switching functions from pin 14 of the SG 3526, or from the microcontroller, or from external sources are input directly to the cathode (pin 3) of a single-channel, high-speed, logic gate optocoupler, HCPL 2211. They are also inverted through standard inverters, SN74LS04, and fed to the cathode (pin 3) of another HCPL 2211. Where the required switching function is other than the actual inverted one (e.g., ac-dc, external $H(t)_2$), it is fed directly to the cathode. The anodes (pin 2) of both the optocouplers are pulled high to +5 V (pin 18 of the SG 3526) through appropriate series resistors. High-frequency switching diodes, 1N 914, connected across the anode and cathode pins of each optocoupler, serve as a protection for the light emitting diode inside the optocoupler. Two different isolated power supplies supply these two optocouplers. The isolated output from pin 7 of

each optocoupler is then fed individually to a high-current buffer, DS 0026 CN, also supplied from the same isolated power supply as its respective optocoupler. The DS 0026 CN is a high-speed, dual-channel interface circuit which accepts standard TTL outputs and converts them to MOS logic levels. Only one channel in each buffer is used. As a MOSFET driver, the output of each buffer varies from 0 to about 11 V, which is then applied directly to the gates of the bilateral switches.

The next step is the design of the two isolated power supplies for the two sets of optocouplers and high-current buffers. This is again described in two steps: the isolated flyback converter and the associated gate drive circuit. The isolated supply for each gate drive consists of a flyback converter. A basic isolated flyback converter is depicted in Figure A.16. The converter used in the actual circuit employs two output windings instead of one, to supply two different sets of optocouplers and high-current buffers. This is one of the advantages of using an isolated flyback converter, where it is possible to have multiple outputs with one input.

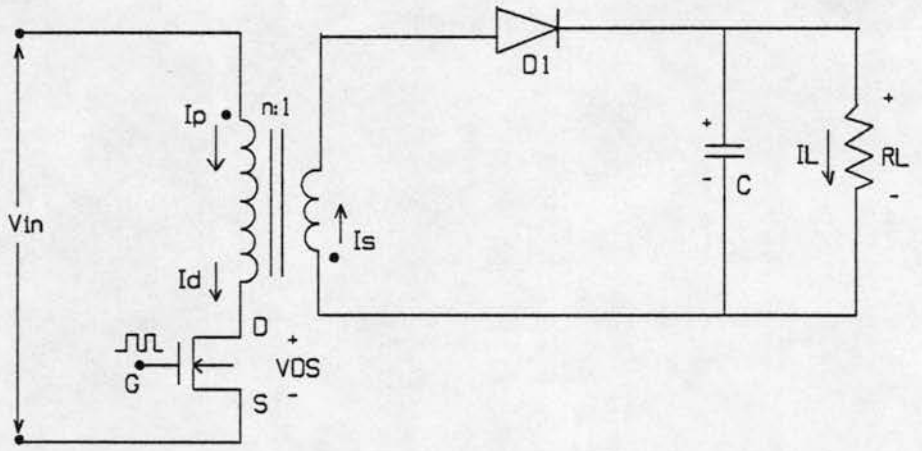


**Figure A.16 A Basic Isolated Flyback Converter Circuit**

The following procedure is used to design the isolated flyback converter [38]:

For transistor $Q_1$, at turn-off

$$V_{DSmax} = \frac{V_{IN}}{1 - D_{max}} \quad ; \quad D\text{-DutyCycle}$$

For a maximum of a 50% duty cycle, $V_{DSmax}=2(V_{IN})$. For an input voltage of +15 V, a transistor with a maximum drain-source voltage of 30 V or greater has to be selected. The IRF 520 (n-channel MOSFET) which has a maximum $V_{DS}$ of 100 V, $R_{DSon}$ of 0.3 Ω and $I_{Dmax}$ of 8.0 A, is found suitable. Its threshold gate-source voltage lies between 2 to 4 V, with a breakdown at 20 V. The next step is the design of the flyback inductor.

The converter is intended to supply the optocoupler, HCPL 2211, and the high-current buffer, DS 0026 CN. An experimental measurement showed that for a switching frequency of about 50 kHz at a 50% duty cycle, the two devices together consume a peak current of about 150 to 200 mA at 11 V. Choosing a higher value of about 450 mA, at an output voltage of 11 V, the output power of the converter turns out to be 5 W for one power supply. Two such supplies (for complementary switching functions) require $P_{OUT}$=10 W.

The transformer peak primary current $I_{PP}$ is given as

$$I_{PP} = \frac{2P_{OUT}}{V_{INmin} D_{max}}$$

Taking the maximum variation in $V_{IN}$ as ±1 V, $I_{PP}$=2.86 A. This is also the peak drain current, which is less than the maximum value of 8.0 A specified for the IRF 520.

For a given variation in $V_{IN}$,

$$D_{min} = \frac{D_{max}}{(1 - D_{max})K + D_{max}} \quad ; \quad K = \frac{V_{INmax}}{V_{INmin}}$$

yielding $K$=1.143 and $D_{min}$=0.147.

The transformer primary inductance is given as

$$L_P = \frac{V_{INmin} D_{max}}{I_{PP} f_{sw}}$$

yielding $L_P$≈49 μH at a switching frequency of 50 kHz.

Assuming an average current density of 400 cir.mils(c.m.)/A, that is, a value of about ($1.27 \times 10^6$/400 A/m$^2$), we have 400x2.86=1144 c.m. This gives a 20 AWG wire, of insulated diameter Dm=0.0351″.

At 25° C, $B_{SAT}$=3800 G, $\mu_i$=750, $B_{max}$=$B_{SAT}$/2=1900 G [39]. Choose a Ferroxcube 3D3 ferrite pot core (2616 PA 250-3D3) and check if the dimensions of the core satisfy the requirements.

The product of the winding area $A_c$ and the core area $A_e$ is given as

$$A_c A_e = \frac{[(25.32) L_P I_{pp} Dm^2] 10^8}{B_{max}}$$

yielding $A_c A_e$ as 0.23 cm$^4$. For the chosen core, $\mu_e$=78, $A_e$=0.948 cm$^2$, and $A_c$=0.4065 cm$^2$. This gives the product $A_c A_e$ as 0.3853 cm$^4$ which is a little higher than the required value of 0.23 cm$^4$.

The effective ungapped core volume $v_e$ is given as

$$v_e = \frac{(0.4\pi) 10^8 (L_P I_{pp}^2)}{B_{max} H}$$

yielding $v_e$ as 53.02 cm$^3$. For the given core, the effective core volume is 3.53 cm$^3$, which is much smaller. The air gap length is 0.04 cm while the required air gap length is

$$l_g = \frac{(0.4\pi L_P I_{pp}^2) 10^8}{B_{max} H}$$

which gives $l_g$=0.0146 cm.

The number of primary turns in the transformer is given as

$$N_P = \frac{B_{max} l_g}{0.4\pi I_{pp}}$$

yielding $N_P \approx 22$.

The number of turns in the secondary winding is given as

$$N_S = \frac{N_P(V_{OUT}+V_D)(1-D_{max})}{V_{INmin} D_{max}} \quad ; \quad V_D = \textit{diode drop (about 1 V)}$$

yielding $N_S \approx 18$. For a maximum secondary current of 450 mA, with a current density of 400 c.m./A, the size of the secondary wire turns out to be 28 AWG.

In practice, the above core turned out to be a little smaller; hence, the next bigger available core (3622 PA 400-3B9) was used. The final design of this flyback inductor is shown in Figure A.17.

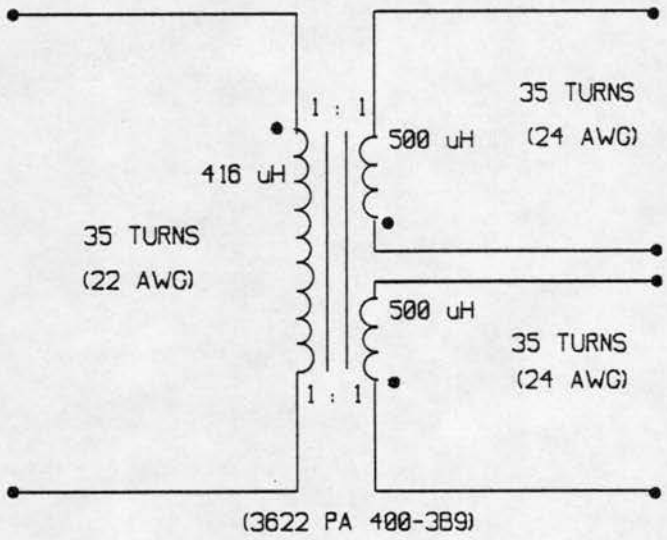


**Figure A.17 Design Of Flyback Inductor**

Experimental results show that with a current limiting resistor (39 Ω, 5 W) added in the primary, the total input current is less than 250 mA, with the output at around 11

V each. A 22 μF capacitor at the output is sufficient to minimize the output ripple to less than 0.2 V peak-to-peak. A 20 μH bead inductance is placed at each output to minimize high-frequency switching noise spikes. A 15 V Zener diode at each output also prevents high-voltage (>15 V) spikes.

The second step in the design of the isolated flyback converter involves the design of the gate drive circuit to provide the required switching function at about 50 kHz and 50% duty cycle to the IRF 520. This is achieved with the help of a simple timer circuit, LM 555, configured in the astable mode of operation. The timer receives its supply of +5 V from pin 18 of the SG 3526. The frequency of oscillation is given as $f_{sw}=1/(t_1+t_2)$, where $t_1$ is the charge time (output high) and is given as $0.693(R_A+R_B)C$; and $t_2$ is the discharge time (output low) and is given as $0.693(R_B)C$. Thus, $f_{sw}=1/T=1.44/(RC)$ where $R=R_A+2R_B$. The duty cycle $D$ is given as $R_B/R$. To achieve a 50% duty cycle, $R_B > R_A$. Choose $R_B$=100 kΩ and $R_A$=1 kΩ. This gives $C$=130 pF for a $f_{sw}$=50 kHz.

The duty cycle can have a maximum value of 0.5. To achieve a slightly higher duty cycle so as to increase the output voltage of the isolated power supply, if necessary, a value of (1-$D$) is supplied to the gate through a standard inverter, SN74LS04. The output of the inverter is passed through a high-current buffer, DS 0026 CN, so as to have the power capacity to drive the IRF 520. The DS 0026 is also supplied by the same +5 V supply as the LM 555. Since the negative supply pin is grounded, the maximum input for the DS 0026 is +5.5 V; hence the supply to LM 555 should not exceed +5.5 V. The output of the DS 0026 is then connected to the gate of IRF 520.

The third and the last step in the design and construction of the gate drive circuit is the implementation of high-power bilateral switches. Two, fast switching, n-channel MOSFETs (MTH 15N35) are placed in series for one bilateral switch. These transistors are

capable of blocking up to 400 V ($V_{DSmax}$), and can conduct up to 15 A of current ($I_{Dmax}$), with an on-state resistance of 0.3 Ω ($R_{DSon}$). The threshold gate-source voltage is between 2 and 4.5 V, with a breakdown at 18 V. A MOSFET has an anti-parallel diode connected across it, by virtue of its architecture. Still, a high-power (30 A, 400 V) ultrafast diode $D_2$ (MUR 3040 PT) is connected across each MOSFET as shown, due to its high speed (35-60 nsec recovery time). Eighteen volt Zener diodes are connected across the gate and source of each MOSFET for overvoltage protection. Fifteen ampere fuses are placed in series with each switch for overcurrent protection. In addition, a standard snubber circuit with values as depicted is placed across the terminals of each MOSFET to snub high-voltage transients during switching, and to minimize commutation losses. This circuit acts directly on the switching trajectory and alters it. Its performance is best achieved if it is wired directly on the switch terminals. The operation of the snubber circuit is described briefly below.

During switch turn-off, the capacitor $C_1$ prevents a sudden change in voltage (for example, when $V=L(di/dt)$). It charges through the fast switching diode $D_1$ (1N 914). Some of the energy needed by the load during commutation is provided by the capacitor. During turn-on, the capacitor discharges through the resistor and the transistor. The small bead inductance $L_1$ prevents a sudden change in current (for example, when $i=C(dv/dt)$).

Thus, two sets of bilateral switches are now available for complementary switching functions. The above gate drive circuit is separate for each phase; hence, there are three such circuits for three different phases. The bilateral switches are mounted in a separate box, as described in Appendix B.

# APPENDIX B

# MANUAL

This Appendix describes a detailed manual for the test bed as built. Photographs and maps are displayed. Several hardware and software details are covered.

## B.1 Layout Photographs

The photographs and maps shown in Figures B.1 through B.7 depict the layout of the test bed. The notation used to denote each part in the photographs is as follows:

x, y part name or function , where x is the horizontal axis coordinate, and y is the vertical axis coordinate.

The coordinates mark the center of any component or block. If the borders of a block are represented, the following notation is used for x and y:

(u-l) ; where u is the upper (left) limit of the block, and l is the lower (right) limit of the block. The components of each board are listed with reference to the figures in Appendix A.

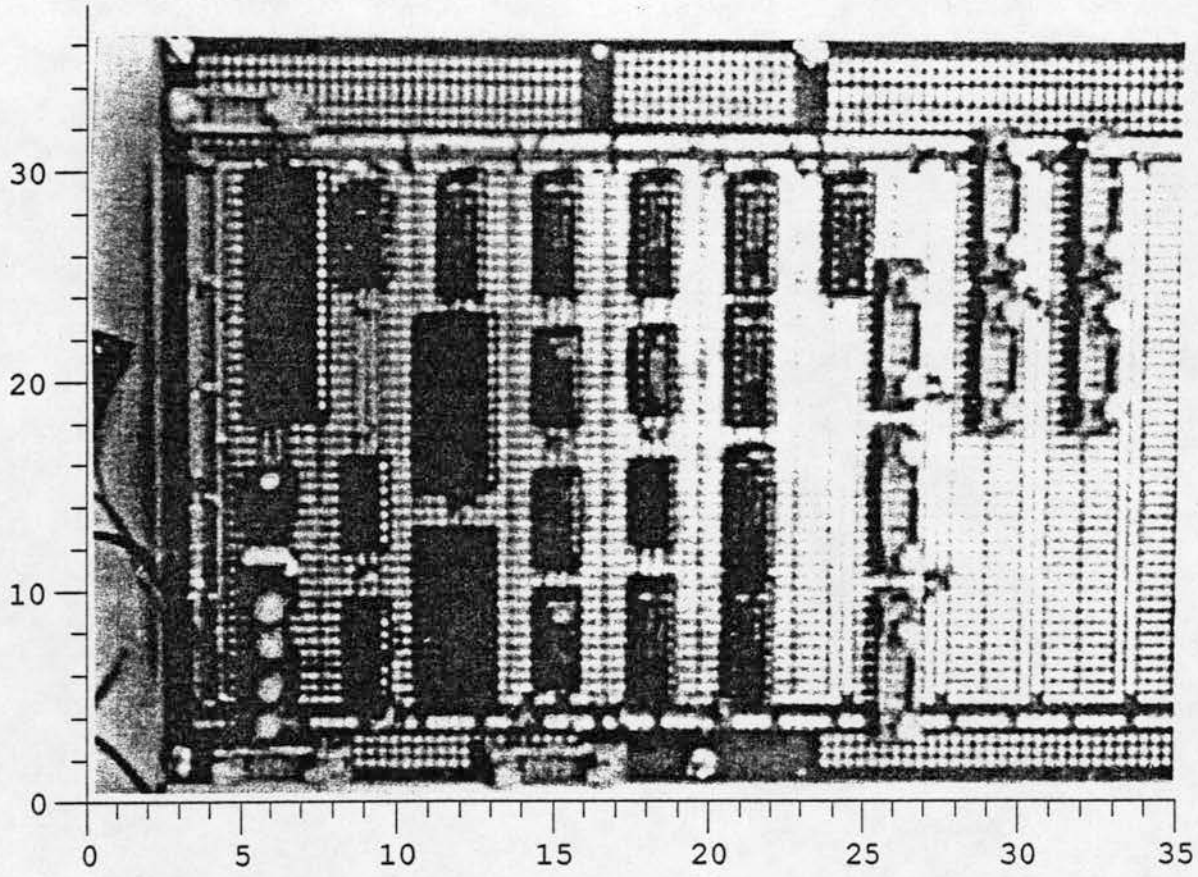


**Figure B.1 Layout Grid for Digital Circuit Board**

Refer to Figure A.1

| | | | |
|---|---|---|---|
| 1, 21 | RS 232 25-pin connector | 15, 1 | J7-1 |
| 5, 33 | J9-1 | 18, 27 | dc-ac frequency latch |
| x-axis, 31.8 | Ground bus | 18, 21 | Inverters (decoder 16-32 K) |
| 6.5, 24 | Microprocessor | 18, 15 | Inverters (decoder 32-48 K) |
| 6, (16-12) | Reset and crystal circuit | 18, 8 | Extra latch ($P_1$) (no enable) |
| 6, (10-4) | RS 232 capacitors | 21, 27 | Triangle amplitude latch |
| 6, 1 | J8-1 | 21, 21 | ac-dc latch |
| 9, 27 | $P_0$ pull-up resistors | 21, 14 | Feedback reference latch |
| 9, 14 | AND gates used on board | 21, 7 | Extra latch ($P_1$) (36-38 K) |
| 9, 7 | RS 232 | 24.5, 27 | Sine wave gain latch |
| 12, 27 | Address-data latch | 26,23 | J1-1 |
| 12, 20 | 0-8 K RAM | 26, 14 | J2-1 |
| 12, 8 | 8-16 K RAM | 26, 7 | J3-1 |
| 15, 27 | dc-dc latch | 29.5, 29 | J4-1 |
| 15, 20 | Decoder (16-32 K) | 29.5, 23 | J5-1 |
| 15, 14 | Decoder (32-48 K) | 32-5, 29 | J6-1 |
| 15, 8 | Decoder (0-64 K) | 32.5, 23 | J10-1 |

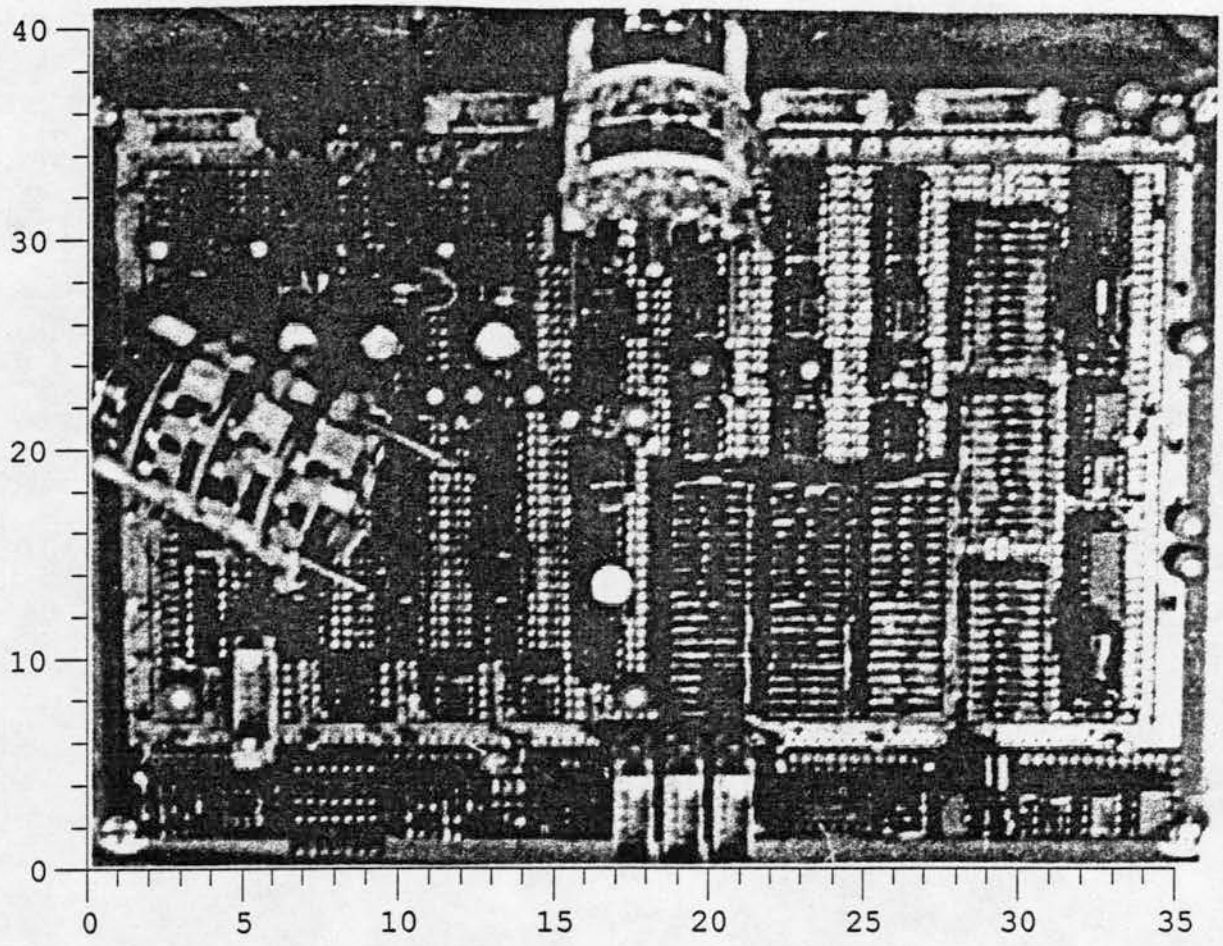


**Figure B.2 Layout Grid for Analog Circuit Board**

The component at coordinates (5, 20) is the ac-dc (Timer Capacitors) rotary switch; at (17, 34) is the VCO resistor and integration capacitor rotary switch. The components below these rotary switches are not visible in Figure B.2, but are given the appropriate coordinates.

| | | | |
|---|---|---|---|
| 1.8, 4.2 | -15 V | 17.5, 3 | J6-2 |
| x-axis, 6.5 | Ground bus | 19, 3 | J7-2 |
| | | 20.5, 3 | J8-2 |

Refer to Figure A.2

| | | | |
|---|---|---|---|
| 3, 8 | $R_1$ | 5, 8 | J1-2 |
| 4, (21-10) | Refer to Figure A.2 | | |

## Analog Circuit Board (continued)

Refer to Figure A.3

| | | | |
|---|---|---|---|
| 3, 35 | J2-2 | 7, (33-10) | Phase A timer circuit |
| 4, (33-22) | DAC circuit | 10, (33-10) | Phase B timer circuit |
| 3, 29 | $R_0$ | 13.5, (33-10) | Phase C timer circuit |

Phase A timer circuit has the following layout (Phases B and C have similar layouts):

| | | | |
|---|---|---|---|
| 7, 32 | Sine to sq. wave comparator | 7, 20 | Timer (C) |
| 5.5, 29 | Comparator 10 kΩ pot. | 7, 17 | Timer (A) |
| 18, 36 | Inverter at timer (B) trigger | 7, 14 | Rotary switch connections |
| 5.5, 22 | Timer (A) phase trim pot. | 7, 11 | Timer (B) |
| 7.5, 22 | Timer (B) phase trim pot. | 4, 8 | Timers A,B output inverters |
| 8, 36 | Timer (C) output inverter (for combinational logic) | 8, 1 | Combinational logic AND gates |

Refer to Figure A.7

| | | | |
|---|---|---|---|
| 16.5, (34-15) | Refer to Figure A.7 | 17.5, 21.8 | VCO supply pot. |
| 15.5, 21.8 | $R_0$ | 13.5, 3 | J3-2 |

Refer to Figure A.9

| | | | |
|---|---|---|---|
| 16.5, 11 | LF 356 (2) | 8.5, 8 | LF 356 (3) |
| 17.5, 8 | Phase adjust pot. $R$ | 5, 3 | LM 311 (1) |
| 14.5, 8 | LM 311 (2) | 2, 16 | LF 356 (1) |
| 11.5, 8 | LM 311 (3) | | |

Refer to Figure A.10

| | | | |
|---|---|---|---|
| 23, 26 | J4-2 | 23, (34-20) | Phase B |
| 20, (34-20) | Phase A | 26, (34-20) | Phase C |

Layout of Phase A is as follows (Phases B and C have similar layouts):

| | | | |
|---|---|---|---|
| 20, 31 | DAC | 20, 24 | Rot. sw. (Cap.) connections |
| 20, 27 | Integration op-amp | 20, 21 | DAC op-amp |

Refer to Figure A.11

| | | | |
|---|---|---|---|
| 20, 13 | Phase A | 29.5, 28 | Phase A |
| 23, 13 | Phase B | 29.5, 20 | Phase B |
| 26, 13 | Phase C | 20.5, 11 | Phase C |

## Analog Circuit Board (continued)

Refer to Figure A.12

| | | | |
|---|---|---|---|
| 28.5, 36 | J5-2 | 33.5, 37 | Phase B $R_3$ (offset) |
| 32.5, 32 | Phase A DAC | 34.5, 3 | Phase B DAC op-amp |
| 32.5, 22 | Phase A offset op-amp | 32.5, 3 | Phase B offset op-amp |
| 32.5, 19 | Phase A DAC op-amp | 34.5-35 | Phase C $R_3$ (offset) |
| 35, 26 | Phase A $R_2$ | 35, 14 | Phase C $R_2$ |
| 32, 35 | Phase A $R_3$ (offset) | 24, 3 | Phase C DAC |
| 32.5, 16 | Phase B DAC | 28, 3 | Phase C offset op-amp |
| 35, 17 | Phase B $R_2$ | 31, 3 | Phase C DAC op-amp |

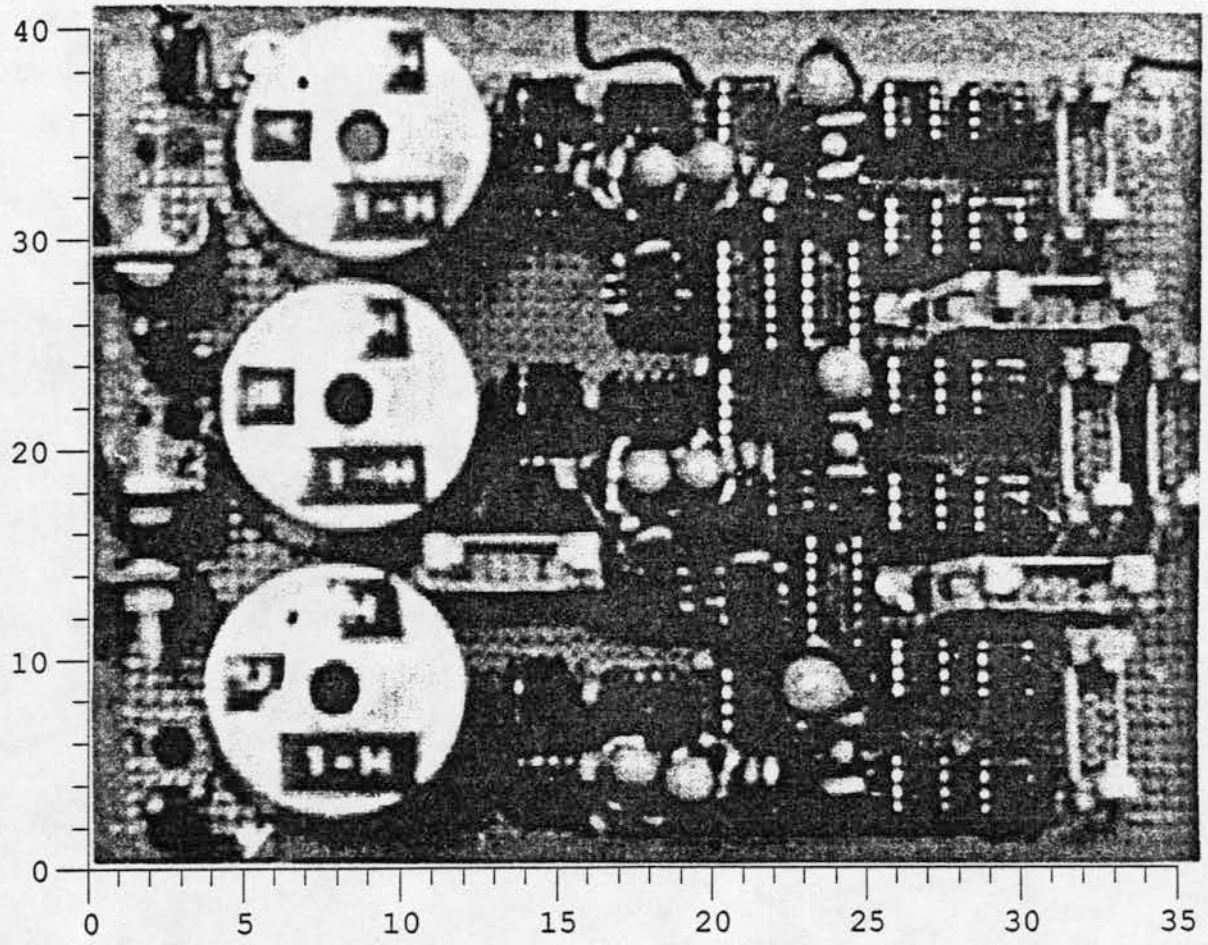


**Figure B.3 Layout Grid for Gate Drive Circuit Board**

| | | | |
|---|---|---|---|
| x-axis, 35 | Phase A | x-axis, 8 | Phase C |
| x-axis, 22 | Phase B | | |

Refer to Figure A.15

Phase A layout is described below (Phases B and C have similar layouts).

| | | | |
|---|---|---|---|
| (0-20), (40-21) | Flyback converter circuit | 24, 12 | Phase C inverters |
| 17, 28 | SG 3526 parts (Freq. cap.) | 32.5, 22 | J3-3 |
| 21, 27 | Inverters | 32.5, 7 | J6-3 |
| (21-30), (28-31) | Switching function circuit | 34.5, 22 | J4-3 |
| (25.5-31), 36 | $H(t)$ | 31.5, 28 | J2-3 |
| (25.5-31), 32 | $1\text{-}H(t)$ | 31.5, 13 | J5-3 |
| 32.5, 35 | J1-3 | 13.5, 15 | J7-3 |
| 2, 34 | +15 V | 18, 14 | Ph. B 3526 parts (fr. cap.) |
| 19.5, 37 | Ground | 21.5, 13 | Ph. C 3526 parts (fr. cap.) |
| 24, 27 | Phase B inverters | 33.5, 38 | +5 V |

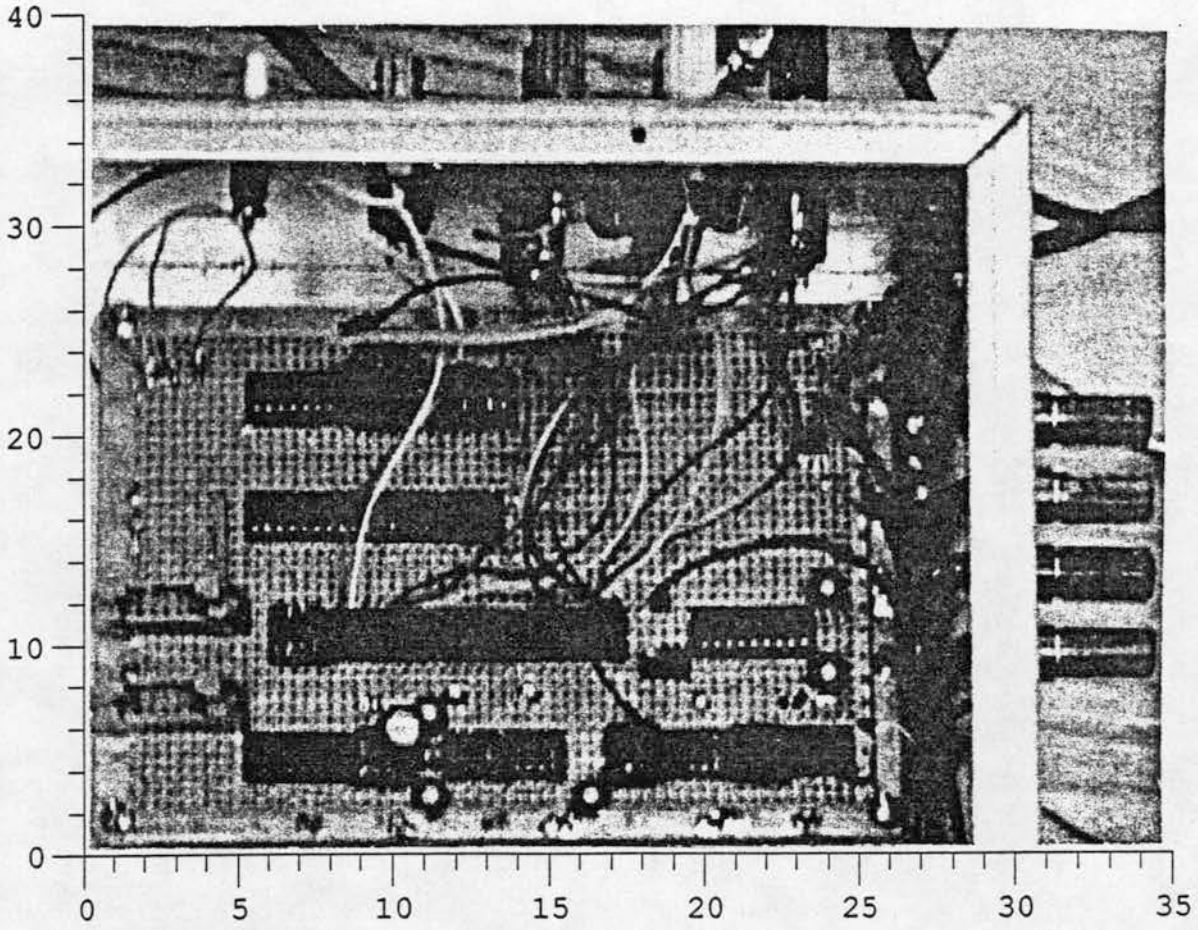


**Figure B.4 Layout Grid for Feedback Circuit Board**

| | | | |
|---|---|---|---|
| x-axis, 1 | Ground bus | 33, 9 | +5 V supply |
| 3, 3 | +15 V bus | 33, 14 | Ground |
| (5-24), 8 | -15 V bus | 33, 17 | -15 V supply |
| 18.5, 12 | +5 V | 33, 21 | +15 V supply |

Refer to Figure A.13

| | | | |
|---|---|---|---|
| 3, 7 | J1-4 | 24, 5 | ADC op-amp |
| 3, 12 | J2-4 | 24, 8.2 | $R_2$ |
| 7, 5 | DAC | 24, 12 | $R_3$ |
| 13, 5 | DAC op-amp | 21.5, 11 | ADC |
| 14.5, 5 | Inverting op-amp | (8-17.5), 11 | Refer to Section B.4 |
| 11, 7 | $R_0$ | 18.5, 9 | $R_A$ |
| 11, 3 | dc reference voltage pot. | 23, 30 | (V) jacks, $R_B$ |
| 16.5, 3 | DAC $V_{REF.}$ pot. | 18, 30 | (I) jacks, $R_C$ |
| 5.5, 31 | ac, dc reference SPDT | 15.5, 30 | (T) jacks, $R_D$ |
| 19.5, 5 | Master op-amp | 10, 30 | Expansion jack, $R_E$ |

## Feedback Circuit Board (continued)

Refer to Figure A.14

| | | | |
|---|---|---|---|
| 7, 16 | data latch | 7, 22 | Inverters |
| 10.5, 16 | (V, I) op-amps | 10, 22 | Op-amp resistors |
| 13, 16 | T, expansion jack op-amps | | |

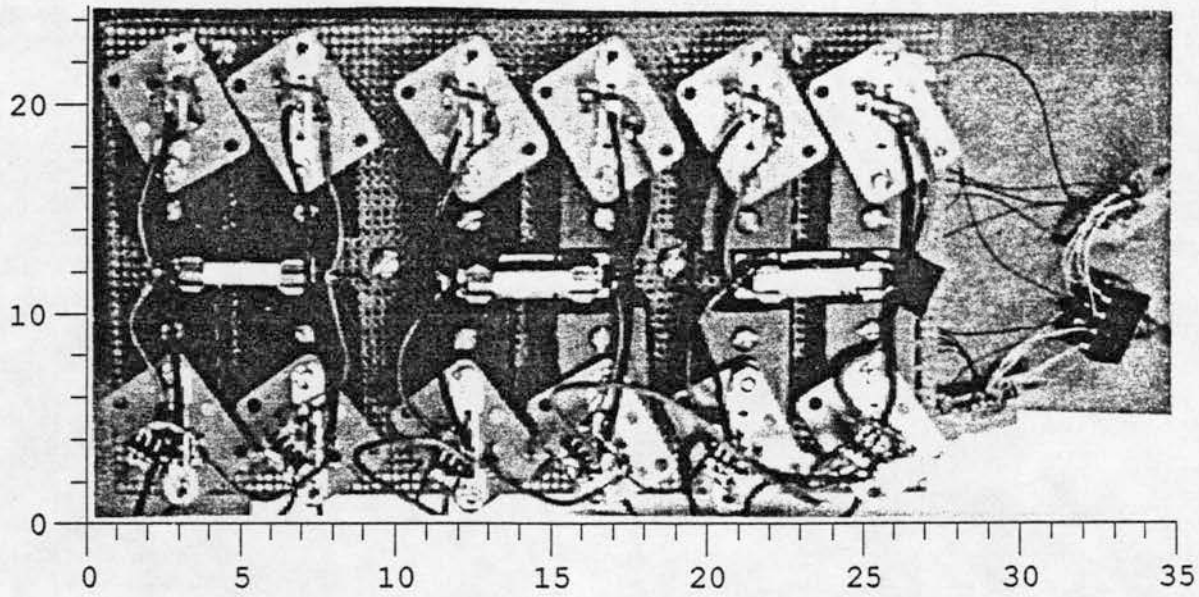


**Figure B.5 Layout Grid for Bilateral Switch Board**

| | | | |
|---|---|---|---|
| 3, 12 | C′; (B′ directly below it) | 33, 9 | Full-bridge switch |
| 14, 12 | C; (B directly below it) | 33.5, 14 | J4-3 |
| 5, 12 | A′; (A directly below it) | 28.5, 5 | J7-3 |

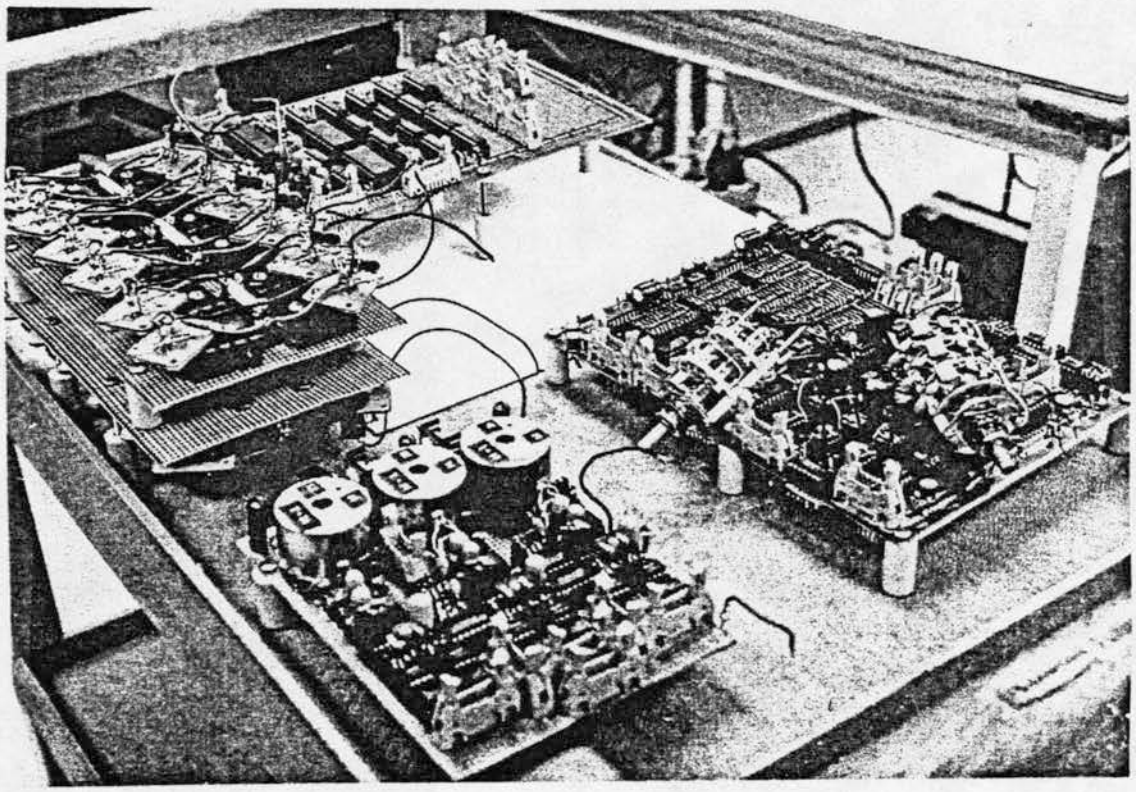

**Figure B.6 Overall Appearance of Different Boards**

Figure B.6 shows an overall appearance of the digital, analog, gate drive and bilateral switch boards, in clockwise direction from top.

Figure B.7 shows the layout of the front panel for one phase.

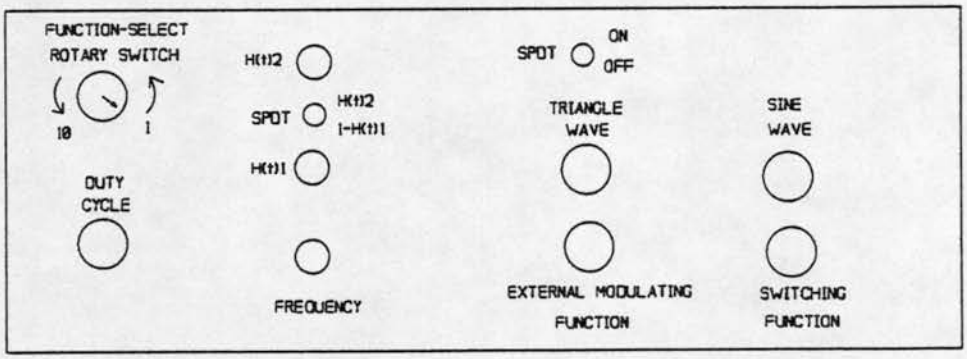


**Figure B.7 Layout of Front Panel for One Phase**

## B.2 Function-Select Rotary Switch Detail

The hardware connections of the function-select rotary switch for each phase are described below.

Each rotary switch on the front panel has 10 positions and 3 wafers. When viewed from the front panel, the positions 1 through 10 are in anti-clockwise direction. The functions of each position are described in Appendix A, Table A.1. The three wafers are numbered I, II and III. Wafer I is the innermost wafer (nearest to the front panel) and III is the outermost (refer to Appendix A, Figure A.15). When viewed from the back of the switch, the hardware configurations of each wafer appear as shown in Figure B.8. The letters "uP" at any position imply that there is an input (switching or modulating function) to that pin from the analog circuit board (board 2). Position 10 is the common position for all pins in each wafer.

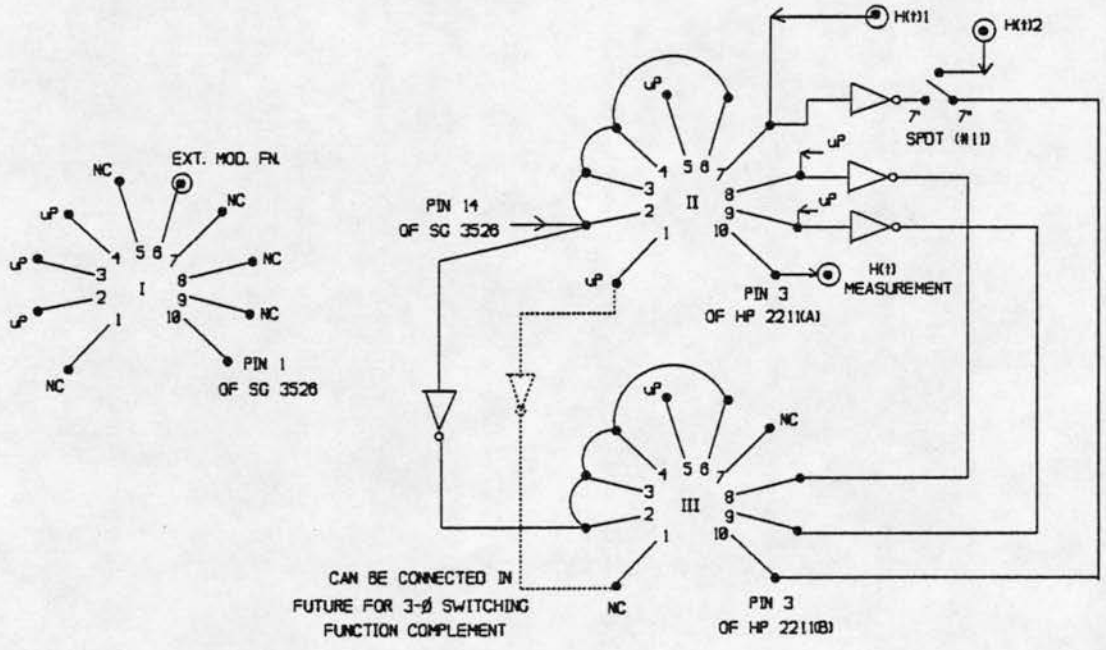


**Figure B.8 Function-Select Rotary Switch Connections**

## B.3 Jumper Connections Detail

Table B.1 describes the connections for each jumper. The connectors are 10-pin flat-ribbon edge connectors. The following notation is used to denote the jumpers:

Jx-y ; where J denotes that it is a jumper,

x denotes the jumper number,

and y denotes the board number.

There are a total of four boards. Hence y can have one of the following values:

1 Digital circuit board.

2 Analog circuit board.

3 Gate drive circuit board.

4 Feedback circuit board.

The values of x and y for the connectors mounted on the main box are the same as for those to which they are connected, on the respective board.

Since the "key" to each male and female socket of the connectors is not available, it is important that they be inserted properly. Figure B.9 shows the proper connection.

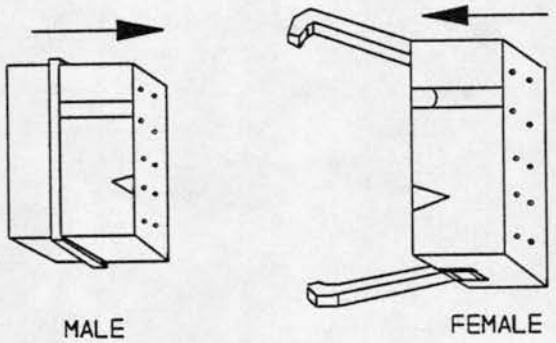


**Figure B.9 Proper Connection for the Male and Female Sockets of Each Connector**

**Table B.1 Jumper Connections**

| Jumper | Connects To | Function |
|---|---|---|
| J1-3 | J1-3 on main box | Phase A switching fns. |
| J2-3 | J2-3 on main box | Fr. & D. pots. for ph. A,B |
| J3-3 | J3-3 on main box | Phase B switching fns. |
| J4-3 | J4-3 on bilateral sw. box | MOSFET sources |
| J5-3 | J5-3 on main box | Fr. & D. pots. for ph. C |
| J6-3 | J6-3 on main box | Phase C switching fns. |
| J7-3 | J7-3 on bilateral sw. box | MOSFET gates |
| J1-1 | J1-2 | dc-dc |
| J2-1 | J2-2 | ac-dc |
| J3-1 | J3-2 | Freq. of modulating fn. |
| J4-1 | J4-2 | Ampl. of triangle wave |
| J5-1 | J5-2 | Ampl. of sine wave |
| J6-1 | J1-4 | Feedback (port 1) |
| J7-1 | J2-4 | ADC (port 0) |
| J8-1 | No connection | $P_0$ (future expansion) |
| J9-1 | No connection | $P_1$ (future expansion) |
| J10-1 | No connection | Extra data latch ($P_1$) |
| J6-2 | J6-2 on main box | Ph. A mod. and sw. fns. |
| J7-2 | J7-2 on main box | Ph. B mod. and sw. fns. |
| J8-2 | J8-2 on main box | Ph. C mod. and sw. fns. |

The hardware configuration for each edge connector is described below. The notation used for connectors (J6-2, J7-2, J8-2) and (J1-3, J3-3, J6-3) is as follows:

x y-z ; where x is the pin number of the edge connector,

y is the wafer number of the function-select rotary switch,

and z is switch position on wafer y.

The order of pins (value of x) in each edge connector is consistent for all. This is shown in Figure B.10.

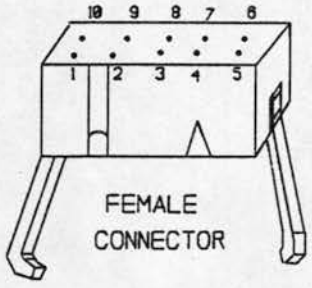


**Figure B.10 Pin Order in Each Edge Connector**

**Connectors J6-2, J7-2 and J8-2 on Main Box**

| | | | |
|---|---|---|---|
| 1 | I-2 | 6 | II-8 |
| 2 | I-3 | 7 | II-9 |
| 3 | I-4 | 8 | III-5 |
| 4 | Front panel jack (sine wave) | 9 | II-1 |
| 5 | II-5 | 10 | Front panel jack (triangle wave) |

**Connectors J1-3, J3-3 and J6-3 on Main Box**

| | | | |
|---|---|---|---|
| 1 | II-6 | 6 | II-9 |
| 2 | II-7 | 7 | II-10 |
| 3 | II-7′ | 8 | III-6 |
| 4 | II-7″ (or III-10) | 9 | III-8 |
| 5 | II-8 | 10 | III-9 |

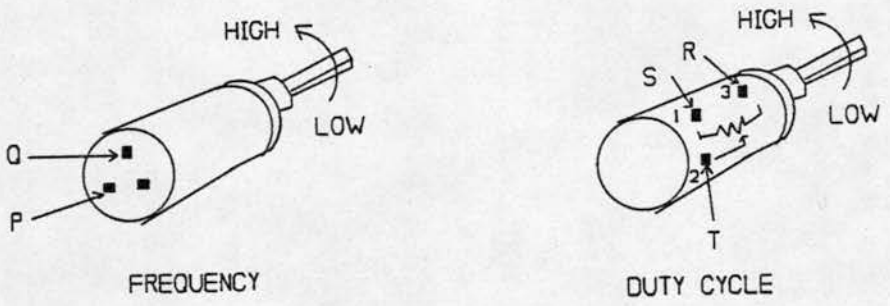


**Figure B.11 Frequency and Duty Cycle Potentiometers**

The connections for the switching frequency and duty cycle potentiometers are shown in Figure B.11. The respective edge connector configurations in Table B.2.

**Table B.2 Connector Details for Frequency and Duty Cycle Potentiometers**

| J5-3 Ph. C Pins | J2-3 Ph. A Pins | J2-3 Ph. B Pins | Connects To |
|---|---|---|---|
| 1 | 1 | 10 | P, pin 9 of Sg 3526 |
| 2 | 2 | 9 | Q, 220 Ω resistor for sw. frequency (at pin 9, SG 3526) |
| 3 | 3 | 8 | R, 1 kΩ resistor (to ground) (at pin 1, SG 3526) |
| 4 | 4 | 7 | S, 1 kΩ resistor (to +5 V) (at pin 1, SG 3526) |
| 5 | 5 | 6 | T, pin 1 of SG 3526 |

**Connectors from Board 1 to Board 2, and from Board 1 to Board 4**

Pins 1 through 8 for J1-1 through J1-5 connect the respective data latches on board 1 to multiplying DACs on board 2.

| J1-1 | | J2-1 | |
|---|---|---|---|
| 1 through 8 | LSB through MSB (dc-dc) | 1 through 8 | LSB through MSB (ac-dc) |
| 9 | NC | 9 | NC |
| 10 | +5 V | 10 | +5 V |

**J3-1**

| | |
|---|---|
| 1 through 8 | LSB through MSB (modulating fn. freq.) |
| 9 | NC |
| 10 | +5 V |

**J4-1**

| | |
|---|---|
| 1 through 8 | LSB through MSB (amplitude of triangle wave) |
| 9 | NC |
| 10 | Phase A sine wave after diode waveshaping, on board 2; pin 10 of J6-1 on board 1 |

**J5-1**

| | |
|---|---|
| 1 through 8 | LSB through MSB (Amplitude of sine wave) |
| 9 | NC |
| 10 | +5 V |

**J6-1**

| | |
|---|---|
| 1 through 8 | LSB through MSB (feedback reference) |
| 9 | enable signal (34-36 K); AD 7574, pin 16 |
| 10 | pin 10 of J4-1; SPDT on back panel (pin 14, DAC) |

**J7-1**

| | |
|---|---|
| 1 through 8 | LSB through MSB (AD 7574 and status monitor latch to port 0) |
| 9 | $\overline{RD}$ from 8052; pin 15 of ADC 7574 |
| 10 | enable signal (38-40 K); pin 1 of data latch for status monitor |

**Connectors For Future Expansion**

**J8-1**

| | |
|---|---|
| 1-8 | LSB-MSB, $P_0$ |
| 9, 10 | NC |

**J9-1**

| | |
|---|---|
| 1-8 | LSB-MSB, $P_1$ |
| 9, 10 | NC |

**J10-1**

| | |
|---|---|
| 1-8 | Extra data latch |
| 9, 10 | NC |

The configuration of the edge connectors on the bilateral switch box is shown below. Jumper J7-3 connects pin 7 of both DS 0026 CNs on board 3 to their respective gates; J4-3 connects pin 3 of both DS 0026 CNs on board 3 to their respective sources.

**Connectors J4-3 and J7-3**

| | | | |
|---|---|---|---|
| 1 | $\bar{C}$ | 6 | A |
| 2 | C | 7 | NC |
| 3 | $\bar{B}$ | 8 | NC |
| 4 | B | 9 | NC |
| 5 | $\bar{A}$ | 10 | NC |

## B.4 Feedback Operational Amplifier Detail

The connections for the quad operational amplifier MC 34084 on board 4 are shown in Figure B.12 (refer to Figure A.13).

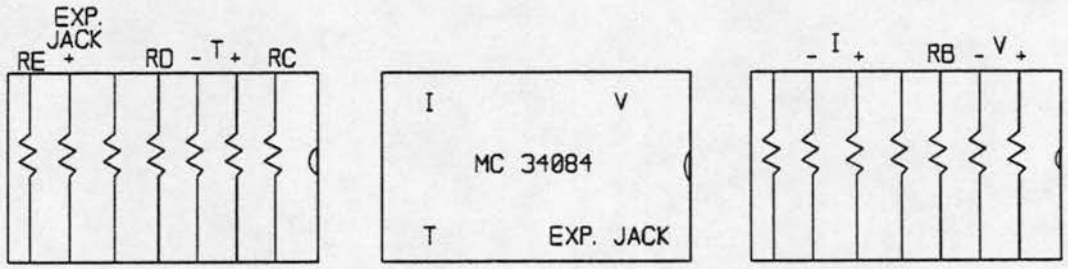


**Figure B.12 Connections for Feedback Quad Operational Amplifier**

## B.5 Full-Bridge Switch Detail

The four-pole, triple-throw switch on the bilateral switch box (for full-bridge converters) has the hardware configuration shown in Figure B.13.

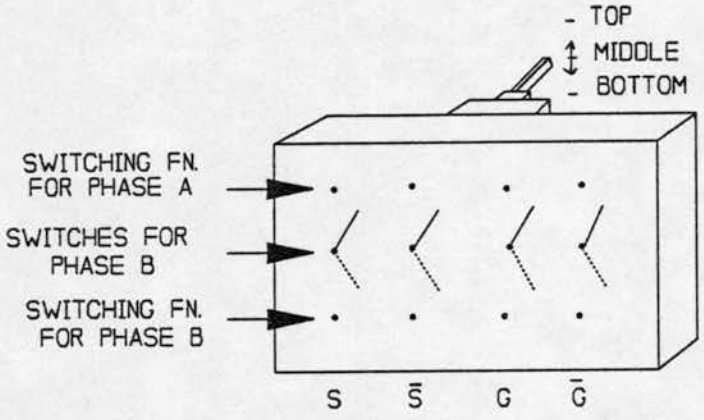


**Figure B.13 Full-Bridge Switch Connections**

When the switch position is on the top, it connects the lower two rows. The switching function for phase B is connected to switches for phase B (normal position).

When the switch position is on the bottom, it connects the upper two rows. The switching function for phase A is thus also connected to switches for phase B (full-bridge position).

When the switch position is in the middle, switches for phase B receive no switching function.

## B.6 Hardware and Software Details

Some important hardware and software details are presented below.

- If the transfer of files from the PC to the system is not proper (characters become distorted), try decreasing the value of the 3 kΩ pull-up resistors at port 0.

- The number of enable signals could be increased (to expand the system) by having increments of 1 K rather than 2 K (from 16-48 K). The upper two signals (48-56 K, 56-64 K) could also be used with additional decoders.
- The 1.8 kΩ resistors used at the trigger pins in timers A and B in ac-dc conversion are placed on the wire-wrap side due to lack of space.
- $X_A'$, $X_B'$ and $X_C'$ (complements of phase delayed, three-phase switching functions) are not available at present.
- To obtain a switching frequency in the range of 0 to 10 kHz, increase the value of the 0.002 μF capacitor at pin 10 of the SG 3526 to about 0.1 μF.
- If the biasing arrangement of the ADC in the "complementary offset binary mode" needs to be changed, refer to the data sheets for the AD 7574.
- The ac reference signal for the DAC 0808 (pin 14) on board 4 is the phase A sine wave (after diode waveshaping, +8.3 V to -8.3 V), and is connected through the following path:

  Phase A sine wave → (J4-2, pin 10) → (J4-1, pin 10) → (J6-1, pin 10) → (J1-4, pin 10) → SPDT switch on back panel → DAC 0808.
- Normally, keep the SPDT switch on the front panel (for each phase) on $H(t)_2$ (top position), and not on $H(t)_1$ (bottom position) unless otherwise required.
- The On/Off SPDT switch for each phase on the front panel controls the +15 V supply to board 4. Always put the switches on only after the program is transferred and running.
- Positions 3 and 4 on each function-select rotary switch are connected to each other (PWM for dc-ac and ac-ac). One position can be disconnected if needed in the future. Each rotary switch actually has 12 positions. Only 10 are used at present.

- There is no protection at present on the +15 V, -15 V and +5 V supply jacks. The supply has to be accurate within ±0.1 V. At present the power input to the system is (+15 V, 600 mA), (-15 V, 250 mA) and (+5 V, 550 mA). If there are separate switches for each supply, first put on the +5 V supply, then the other two. Put them off in the reverse order.
- Remember to attach the male and female sockets of each edge connector properly, since the "key" for these is not available.
- The SG 3526 and the LM 555 are not linear, hence there may be some discrepancies in the switching functions.
- Bypass capacitors (0.01 μF or 0.1 μF) are connected all over the boards on the wire-wrap side. A short circuit on one of the supplies may be due to damage to or dislodging of one of these.

  Some details about the serial communications routine SERCOM.BAS are presented below.
- This program is written with the help of a software package called "Quick Basic." It is stored in a text form readable by other forms of BASIC. To run the program, type QB/RUN SERCOM.BAS. If the system is connected properly, the messages for MCS-BASIC 52: v1.1 will appear on the screen within 2 to 3 seconds. If the program stalls after printing the first line, it may be due to one of the following:

  - RS 232 cable is loose.

  - RS 232 chip is damaged.

  - Improper voltage supply to the digital circuit.
- The 8052 needs the first character transferred as the "space bar" to sign on. This is taken care of by the serial communications routine.

- To exit from the system if it stalls, press Ctrl (Scroll Lock). The +5 V supply to the 8052 has to be shut off and put on again to rerun SERCOM.BAS.
- This program stores a small BASIC routine in the memory to transfer HEX files. This routine starts from line 60000 onwards. To run this routine, type GOTO 60000.
- Keep all statement numbers for any program as less than 60000. Put an END statement at the end of each software file, since all files are concatenated when stored in the memory.
- During the run, typing SAVE will save the software file present in the system RAM, in a file called TEMP.BAS on the PC. The software file is scrolled on the screen as it is saved. If it stops scrolling in case of huge files, the latter part is not saved. The software can be modified to do this.

### B.7 List of Chips

Some of the important silicon chips used in the test bed are listed below.

| | | |
|---|---|---|
| SN74LS373N | LF 356 | SG 3526N |
| SN74LS08N | LM 393 | HP 2211 |
| SN74LS04N | LM 311 | DS 0026CN |
| SN74LS138N | LM 555 | MTH 15N35 |
| DAC 0808 | LM 566 | IRF 520 |
| DAC 1020LCN | TSC RS 232 | MUR 3040PT |
| AD 7574 | INTEL 8052AH-BASIC | |

# APPENDIX C

# SOFTWARE

This Appendix provides the necessary software for power conversions in all four quadrants of the voltage-current axes.

```
' (SERCOM.BAS)          ... RAJIV K. BAPHNA   ;  MAY 15, 1990.
' THIS PROGRAM IS MEANT TO PROVIDE COMMUNICATION OF
' SOFTWARE WITH THE 8052-AH BASIC SYSTEM , THROUGH I/O PORT  COM1:,
' AT A BAUD RATE OF 9600.
'
CLS
'
' OPEN COM1: AS #1 & SOFTWARE FILE AS #2
'
OPEN "COM1:9600,N,8,1,ASC,DS0,RS,RB30000,TB30000" FOR RANDOM AS #1
'
' 8052 NEEDS SPACE-BAR AS FIRST CHAR. TO SIGN ON
'
XOFF$ = CHR$(19)
XON$ = CHR$(17)
'
C$ = CHR$(32)
PRINT #1, C$
PRINT "MCS BASIC-52 : VERSION 1.1 "
'
GOSUB DELAY
PRINT #1, "XTAL=10000000"        'ASSIGN CRYSTAL VALUE TO 8052
GOSUB OUT1
GOSUB MEM
GOSUB OUT1
GOSUB OUT1
'
TI: PRINT
   PRINT "DO YOU WANT TO TRANSFER A FILE (T) OR INTERACT DIRECTLY (I)"
   INPUT "WITH THE 8052-AH BASIC SYSTEM"; L$
   IF L$ = "I" THEN GOTO INP1
   IF L$ = "T" THEN GOTO INP2
   GOTO TI
'
INP2: PRINT
     PRINT "          ***     IMPORTANT     ****
     PRINT
     PRINT "   TRANSFERRING ANY BASIC FILE WILL CLEAR THE MEMORY FILLED"
     PRINT "   UP BEFORE (OTHER THAN BASIC FILES WITH DIFF. LINE NOS.)"
     PRINT "   SO PLEASE TRANSFER ASSEMBLY LANGUAGE FILES ONLY AFTER ALL"
     PRINT "   THE BASIC FILES HAVE BEEN TRANSFERRED !!"
     PRINT "   EDITING ANY BASIC FILE WITH DIRECT INTERACTION WILL  ALSO"
     PRINT "   DELETE ANY STORED HEX. FILE."
     PRINT
 PRINT "IS IT A BASIC (B) FILE OR AN ASSEMBLY LANG.HEX(INTEL FORMAT) FILE (H)"
     INPUT FIL$
     PRINT
     PRINT "INPUT NAME OF FILE TO BE STORED IN THE 8052 EXT. RAM :"
     INPUT F$
     OPEN F$ FOR INPUT AS #2
'
' START INPUTTING SOFTWARE FILE TO 8052 RAM
'
IF FIL$ = "B" THEN GOTO INP3
IF FIL$ = "H" THEN GOTO INP4
CLOSE #2
GOTO INP2
```

```
'
'BASIC FILE
'
INP3: GOSUB DELAY
    DO UNTIL EOF(2)
    LINE INPUT #2, H$
    PRINT #1, H$
    GOSUB OUT1
    LOOP
    CLOSE #2
    GOSUB DELAY
  GOTO STD
'
'ASSEMBLY LANG. HEX FILE (INTEL HEX. FORMAT ONLY!)
'
INP4: PRINT "ENTER ADDR. OF RAM LOCN. TO STORE HEX FILE, IN DECIMAL
DIGITS."
    PRINT "ADDR. HAS TO BE BETWEEN 8193 AND 16384 ONLY."
    INPUT ADRS
    IF (ADRS < 8193) OR (ADRS > 16384) THEN GOTO INP4
'
PRINT : PRINT : PRINT : PRINT : PRINT : PRINT "STORING FILE..PLEASE WAIT.."
PRINT
'
    GOSUB DELAY
    CT = 1
LIN:  LINE INPUT #2, H$              ' READ REC. FROM HEX FILE (INTEL HEX)
    C1$ = MID$(H$, 2, 1): C2$ = MID$(H$, 3, 1)       ' READ REC. LENGTH
    GOSUB DECVAL
    '
    NBYTES = (16 * C1) + C2     ' HEX. TO DECIMAL  (TOTAL DATA BYTES)
    IF NBYTES = 0 THEN GOTO CL2                  ' 0 IS 'END' RECORD
    '
    J = 10      ' STARTING POSITION OF DATA BYTES IN INTEL HEX. FORMAT
    '
    FOR W = 1 TO NBYTES
    ADR = ADRS + W - 1                ' GET ADDRESS OF NEXT LOCATION
    C1$ = MID$(H$, J, 1): C2$ = MID$(H$, J + 1, 1)   ' GET 2 DATA CHARS.
    GOSUB DECVAL
    DAT = (16 * C1) + C2                          ' HEX. TO DECIMAL
    ADR$ = STR$(ADR): DAT$ = STR$(DAT)
    PRINT #1, "GOTO 60000"                ' RUN STORED BASIC ROUTINE
    GOSUB DELAY
    PRINT #1, ADR$
    GOSUB DELAY
    PRINT #1, DAT$
    GOSUB DELAY
    J = J + 2                       ' POSITION OF NEXT 2 DATA CHARS.
    NEXT W
    CT = CT + 1
    IF CT > 1 THEN ADRS = ADRS + NBYTES
  GOTO LIN
  '
CL2: CLOSE #2
STD: PRINT "THE FILE IS NOW LOADED INTO THE 8052-AH BASIC SYSTEM RAM"
  PRINT
  PRINT "YOU MAY INTERACT WITH IT AS USUAL": PRINT
```

```
  '
INP1: PRINT "THE PROMPT SIGN IS GIVEN BY '>>' "
      PRINT
  '
  'INTERACTION WITH 8052 AFTER SOFTWARE FILE IS STORED IN RAM
  '
AGAIN:  PRINT "TYPE 'BREAK' TO STOP A RUN,'END' TO END,'X' TO XFER. NEW
FILE"
      PRINT "TYPING 'SAVE' WILL SAVE THE UPDATED FILE IN TEMP.BAS"
      INPUT ">>", B$                          ' ENTER COMMAND
      IF B$ = "SAVE" THEN GOTO ENOUGH
      IF B$ = "END" THEN GOTO FINISH
      IF B$ = "X" THEN GOTO TI
      IF B$ = "BREAK" THEN B$ = CHR$(3)
      PRINT #1, B$            ' SEND COMMAND, I/P FROM KYBD., TO 8052
      GOSUB DELAY
      '
CHECK1: IF LOC(1) > 6 THEN GOTO OUT2 ELSE GOTO AGAIN
OUT2:   LINE INPUT #1, AE$          ' OUTPUT CONTENTS OF COM1: ON SCREEN
      PRINT AE$
      GOTO CHECK1
      '
      'STORE UPDATED FILE FROM 8052 RAM IN TEMP.BAS
      '
ENOUGH: OPEN "TEMP.BAS" FOR OUTPUT AS #3 LEN = 30000
      GOSUB DELAY
      PRINT #1, "LIST"
      GOSUB DELAY
      LINE INPUT #1, AE$      ' DO NOT STORE TOP LINE WHICH SAYS "LIST"
      '
CHECK2: IF LOC(1) > 15 THEN GOTO SAVE ELSE GOTO AGAIN
SAVE:   LINE INPUT #1, AE$
      PRINT AE$           ' PRINT EACH LINE ON SCREEN AS IT IS SAVED
      PRINT #3, AE$                       ' SAVE IN TEMP.BAS
      GOTO CHECK2
      '
FINISH: GOSUB DELAY                       ' CLOSE FILES AND STOP
      CLOSE #3
      CLOSE #1

      STOP
  '-----------------------------------------------
  ' SUBROUTINES
  '
DELAY:
  FOR I = 1 TO 5000
  I = I + 1
  NEXT I
  RETURN
  '
OUT1:
  FOR I = 1 TO 13000                      ' DELAY
  I = I + 1
  NEXT I
  LINE INPUT #1, AE$              ' READ INPUT TO COM1: FROM 8052
  PRINT AE$                         ' AND PRINT ON SCREEN
  RETURN
```

```
'
MEM: GOSUB DELAY
    PRINT #1, "59999 REM -BASIC ROUTINE TO STORE HEX FILE"
    GOSUB OUT1
    PRINT #1, "60000 INPUT A1"                    ' BASIC ROUTINE IN 8052
    GOSUB OUT1                                    ' TO STORE HEX FILE
    PRINT #1, "60010 INPUT D1"
    GOSUB OUT1
    PRINT #1, "60020 XBY(A1)=D1"
    GOSUB OUT1
    PRINT #1, "60060 END"
    GOSUB OUT1
    RETURN
    '
DECVAL: IF ASC(C1$) < 65 THEN GOTO ACT1        ' CONVERT TO DECIMAL VALUE
       C1 = ASC(C1$) - 55: GOTO CHEC2
ACT1:   C1 = VAL(C1$)
CHEC2:  IF ASC(C2$) < 65 THEN GOTO ACT2
       C2 = ASC(C2$) - 55: RETURN
ACT2:   C2 = VAL(C2$)
       RETURN
       '
    END
```

```
REM   (BUCK.BAS)          ... RAJIV K. BAPHNA  ;  DEC. 1990
REM   THIS IS A DC-DC BUCK CONVERTER WITH A FEEDBACK OPTION FOR VOLTAGE
10    PRINT "DC - DC BUCK CONVERTER"
20    PRINT "FOR O/P VOLTAGES RANGING FROM 0-120 V"
40    PRINT "ENTER INPUT VOLTAGE VIN"
50    INPUT VIN
60    PRINT "ENTER OUTPUT VOLTAGE VO"
70    INPUT VO
80    IF 0<=VO .AND. VO<=120 .AND. VIN>0 THEN 130
90    IF VIN > 0 THEN PRINT "VO OUT OF RANGE"
100   IF VIN < 0 THEN PRINT "VIN CAN'T BE -VE"
120   GOTO 10
REM   DUTY CYCLE DT FOR #1
130   DT = VO / VIN
140   IF DT <= 1 THEN 170
150   PRINT "FOR BUCK CONV. VO HAS TO BE <= VIN"
160   GOTO 40
REM   CONVERT DT TO DIGITAL VALUE VIA APPROPRIATE FN.
170   FT = 1 - DT
REM   FOLLOWING FN. CAN BE CHANGED AS DESIRED
180   X1 = 225 * FT + 25
190   PRINT "DIGITAL VALUE OF DUTY CYCLE:", X1
200   PRINT "IS IT OPEN(1) OR CLOSED LOOP(2) SYSTEM ?"
210   INPUT SYST
220   IF SYST = 1 THEN 250
230   IF SYST = 2 THEN 310
240   GOTO 200
REM   OUTPUT X1 ON PORT 1
250   FOR P = 1 TO 2
REM   ENABLE DC MOD. LATCH
260   XBY(17000) = 0
270   PORT1 = X1
REM   DISABLE LATCH
280   XBY(15000) = 0
290   NEXT P
300   GOTO 760
REM   VOLTAGE FEEDBACK LOOP
310   PRINT "F/B VOLT. FROM CONV. O/P HAS TO BE <=12 V"
320   PRINT "INPUT STEP DOWN FACTOR FOR O/P VOLTAGE :"
330   INPUT S1
340   IF S1 <= 0 THEN 320
REM   CALC. uP REFERENCE (CONSIDERING LINEAR VO v/s X1)
350   RE = (252 * VO) / (12 * S1)
355   IF RE < 0 .OR. RE > 255 THEN PRINT "F/B FACTOR INCORRRECT !":GOTO 310
360   PRINT "uP DIGITAL REFERENCE :", RE
REM   OUTPUT X1 ON PORT 1 TO DC MOD. LATCH
370   FOR P = 1 TO 2
380   XBY(17000) = 0
390   PORT1 = X1
400   XBY(15000) = 0
410   NEXT P
REM   OUTPUT RE ON PORT 1 TO F/B LATCH
420   FOR P = 1 TO 2
430   XBY(33000) = 0
440   PORT1 = RE
450   XBY(15000) = 0
460   NEXT P
```

```
470     PRINT "INCREASE VIN SLOWLY"
480     PRINT "ADJUST ALL F/B POTS, CONNECT VOLTAGE F/B"
490     PRINT "WHEN DONE, ENTER ANY NUMBER AND C/R :"
500     INPUT TEMP
REM     START A/D CONVERSION FOR ERROR
510     XBY(48000) = 0
REM     CONVERSION DELAY
520     FOR J = 1 TO 20: J = J + 1: NEXT J
REM     STORE ERROR IN E1
530     E1 = XBY(48000)
540     XBY(15000) = 0
REM     CHECK FOR NEAR-ZERO ERROR
550     IF E1<131 .AND. E1>125 THEN GOTO 510
REM     PROPORTIONAL CONTROL
570     X1 = X1 + (E1 - 128) / 4
REM     CHECK FOR MIN. AND MAX. DUTY CYCLE VALUES
580     IF X1 > 20 THEN 630
600     PRINT "HIGHEST D; NO MORE CONTROL POSSIBLE !"
REM     FIX MAX. VALUE FOR DUTY CYCLE
610     X1 = 30
620     GOTO 700
630     IF X1 < 250 THEN 700
640     PRINT "LOWEST D; NO MORE CONTROL POSSIBLE !"
REM     FIX MIN. VALUE FOR DUTY CYCLE
650     X1 = 250
REM     OUTPUT X1 ON PORT 1 TO DC MOD. LATCH
700     FOR P = 1 TO 2
710     XBY(17000) = 0
720     PORT1 = X1
730     XBY(15000) = 0
740     NEXT P
750     GOTO 510
760     STOP
770     END
```

```
REM   (BOOST.BAS)          ... RAJIV K. BAPHNA  ;  DEC. 1990
REM   THIS IS A DC-DC BOOST CONVERTER WITH A FEEDBACK OPTION FOR VOLTAGE
10    PRINT "DC - DC BOOST CONVERTER"
20    PRINT "FOR O/P VOLTAGES RANGING FROM VIN TO (2.5)VIN"
40    PRINT "ENTER INPUT VOLTAGE VIN (<= 120 V.)"
50    INPUT VIN
60    PRINT "ENTER OUTPUT VOLTAGE VO"
70    INPUT VO
80    IF 0<=VIN .AND. VIN<=120 .AND. VO>0 THEN 130
90    IF VO > 0 THEN PRINT "VIN OUT OF RANGE"
100   IF VO < 0 THEN PRINT "VO CAN'T BE -VE"
120   GOTO 10
REM   DUTY CYCLE D2 FOR #2
130   D2 = VIN / VO
REM   KEEP DUTY CYCLE FOR #2 LESS THAN 60%
140   IF D2 > .4 .AND. D2 <= 1 THEN 180
150   PRINT "KEEP VO <= (2.5)VIN"
160   GOTO 40
REM   CONVERT D2 TO DIGITAL VALUE VIA APPROPRIATE FN.
REM   FOLLOWING FN. CAN BE CHANGED AS DESIRED
180   X1 = 210 * D2 + 10
190   PRINT "DIGITAL VALUE OF DUTY CYCLE:", X1
200   PRINT "IS IT OPEN(1) OR CLOSED LOOP(2) SYSTEM ?"
210   INPUT SYST
220   IF SYST = 1 THEN 250
230   IF SYST = 2 THEN 310
240   GOTO 200
REM   OUTPUT D2 ON PORT 1
250   FOR P = 1 TO 2
REM   ENABLE DC MOD. LATCH
260   XBY(17000) = 0
270   PORT1 = X1
REM   DISABLE LATCH
280   XBY(15000) = 0
290   NEXT P
300   GOTO 760
REM   VOLTAGE FEEDBACK LOOP
310   PRINT "F/B VOLT. FROM CONV. O/P HAS TO BE <=12 V"
320   PRINT "INPUT STEP DOWN FACTOR FOR O/P VOLTAGE :"
330   INPUT S1
340   IF S1 <= 0 THEN 320
REM   CALC. uP REFERENCE (CONSIDERING LINEAR VO v/s X1)
350   RE = (252 * VO) / (12 * S1)
355   IF RE < 0 .OR. RE > 255 THEN PRINT "F/B FACTOR INCORRECT !":GOTO 310
360   PRINT "uP DIGITAL REFERENCE :", RE
REM   OUTPUT X1 ON PORT 1 TO DC MOD. LATCH
370   FOR P = 1 TO 2
380   XBY(17000) = 0
390   PORT1 = X1
400   XBY(15000) = 0
410   NEXT P
REM   OUTPUT RE ON PORT 1 TO F/B LATCH
420   FOR P = 1 TO 2
430   XBY(33000) = 0
440   PORT1 = RE
450   XBY(15000) = 0
460   NEXT P
```

```
470     PRINT "INCREASE VIN SLOWLY"
480     PRINT "ADJUST ALL F/B POTS, CONNECT VOLTAGE F/B"
490     PRINT "WHEN DONE, ENTER ANY NUMBER AND C/R :"
500     INPUT TEMP
REM     START A/D CONVERSION FOR ERROR
510     XBY(48000) = 0
REM     CONVERSION DELAY
520     FOR J = 1 TO 20: J = J + 1: NEXT J
REM     STORE ERROR IN E1
530     E1 = XBY(48000)
540     XBY(15000) = 0
REM     CHECK FOR NEAR-ZERO ERROR
550     IF E1<132 .AND. E1>124 THEN GOTO 510
REM     PROPORTIONAL CONTROL
570     X1 = X1 + (E1 - 128) / 4
REM     CHECK FOR MIN. AND MAX. DUTY CYCLE VALUES
580     IF X1 > 114 THEN 630
600     PRINT "HIGHEST D; NO MORE CONTROL POSSIBLE !"
REM     FIX MAX. VALUE FOR DUTY CYCLE
610     X1 = 115
620     GOTO 700
630     IF X1 < 250 THEN 700
640     PRINT "LOWEST D; NO MORE CONTROL POSSIBLE !"
REM     FIX MIN. VALUE FOR DUTY CYCLE
650     X1 = 250
REM     OUTPUT X1 ON PORT 1 TO DC MOD. LATCH
700     FOR P = 1 TO 2
710     XBY(17000) = 0
720     PORT1 = X1
730     XBY(15000) = 0
740     NEXT P
750     GOTO 510
760     STOP
770     END
```

```
REM   (BUCBOOST.BAS)      ... RAJIV K. BAPHNA  ;  DEC. 1990
REM   THIS IS A DC-DC BUCK-BOOST CONVERTER WITH A FEEDBACK OPTION FOR VOLTAGE
10    PRINT "DC - DC BUCK-BOOST CONVERTER"
20    PRINT "FOR O/P VOLTAGES RANGING FROM 0 TO (2.5)VIN"
40    PRINT "ENTER INPUT VOLTAGE VIN (<= 120 V.)"
50    INPUT VIN
60    PRINT "ENTER OUTPUT VOLTAGE VO"
70    INPUT VO
80    IF 0<=VIN .AND. VIN<=120 .AND. VO>0 THEN 130
90    IF VO > 0 THEN PRINT "VIN OUT OF RANGE"
100   IF VO < 0 THEN PRINT "VO CAN'T BE -VE"
120   GOTO 10
REM   DUTY CYCLE D1 FOR #1
130   D1 = VO / (VIN + VO)
REM   KEEP DUTY CYCLE FOR #1 LESS THAN 60%-70%
140   IF D1 < 0.77 .AND. D1 >= 0 THEN 170
150   PRINT "KEEP VO <= (2.5)VIN"
160   GOTO 40
REM   CONVERT D1 TO DIGITAL VALUE VIA APPROPRIATE FN.
170   F1 = 1 - D1
REM   FOLLOWING FN. CAN BE CHANGED AS DESIRED
180   IF VO <= VIN THEN X1 = 225 * F1 + 25 ELSE X1 = 220 * F1 + 35
190   PRINT "DIGITAL VALUE OF DUTY CYCLE:", X1
200   PRINT "IS IT OPEN(1) OR CLOSED LOOP(2) SYSTEM ?"
210   INPUT SYST
220   IF SYST = 1 THEN 250
230   IF SYST = 2 THEN 310
240   GOTO 200
REM   OUTPUT X1 ON PORT 1
250   FOR P = 1 TO 2
REM   ENABLE DC MOD. LATCH
260   XBY(17000) = 0
270   PORT1 = X1
REM   DISABLE LATCH
280   XBY(15000) = 0
290   NEXT P
300   GOTO 760
REM   VOLTAGE FEEDBACK LOOP
310   PRINT "F/B VOLT. FROM CONV. O/P HAS TO BE <=12 V"
320   PRINT "INPUT STEP DOWN FACTOR FOR O/P VOLTAGE :"
330   INPUT S1
340   IF S1 <= 0 THEN 320
REM   CALC. uP REFERENCE (CONSIDERING LINEAR VO v/s X1)
350   RE = (252 * VO) / (12 * S1)
355   IF RE < 0 .OR. RE > 255 THEN PRINT "F/B FACTOR INCORRECT !":GOTO 310
360   PRINT "uP DIGITAL REFERENCE :", RE
REM   OUTPUT X1 ON PORT 1 TO DC MOD. LATCH
370   FOR P = 1 TO 2
380   XBY(17000) = 0
390   PORT1 = X1
400   XBY(15000) = 0
410   NEXT P
REM   OUTPUT RE ON PORT 1 TO F/B LATCH
420   FOR P = 1 TO 2
430   XBY(33000) = 0
440   PORT1 = RE
450   XBY(15000) = 0
```

```
460     NEXT P
470     PRINT "INCREASE VIN SLOWLY"
480     PRINT "ADJUST ALL F/B POTS, CONNECT VOL. F/B (WITH CORRECT POLARITY !)"
490     PRINT "WHEN DONE, ENTER ANY NUMBER AND C/R :"
500     INPUT TEMP
REM     START A/D CONVERSION FOR ERROR
510     XBY(48000) = 0
REM     CONVERSION DELAY
520     FOR J = 1 TO 20: J = J + 1: NEXT J
REM     STORE ERROR IN E1
530     E1 = XBY(48000)
540     XBY(15000) = 0
REM     CHECK FOR NEAR-ZERO ERROR
550     IF E1<132 .AND. E1>124 THEN GOTO 510
REM     PROPORTIONAL CONTROL
570     X1 = X1 + (E1 - 128) / 8
REM     CHECK FOR MIN. AND MAX. DUTY CYCLE VALUES
580     IF X1 > 70 THEN 630
600     PRINT "HIGHEST D; NO MORE CONTROL POSSIBLE !"
REM     FIX MAX. VALUE FOR DUTY CYCLE
610     X1 = 70
620     GOTO 700
630     IF X1 < 250 THEN 700
640     PRINT "LOWEST D; NO MORE CONTROL POSSIBLE !"
REM     FIX MIN. VALUE FOR DUTY CYCLE
650     X1 = 250
REM     OUTPUT X1 ON PORT 1 TO DC MOD. LATCH
700     FOR P = 1 TO 2
710     XBY(17000) = 0
720     PORT1 = X1
730     XBY(15000) = 0
740     NEXT P
750     GOTO 510
760     STOP
770     END
```

```
REM   (AC_DC.BAS)          ... RAJIV K. BAPHNA  ; DEC. 1990
REM   THIS PROGRAM PERFORMS OPEN LOOP PHASE DELAY CONTROL
10    PRINT "PHASE DELAY CONTROL"
20    PRINT "ENTER INPUT FREQUENCY (15 - 650 Hz. ONLY) :"
30    INPUT F1
40    IF F1<15 .OR. F1>650 THEN GOTO 20
50    PRINT "ENTER REQD. PHASE DELAY (0 - 180 DEGREES ONLY) :"
60    INPUT PD
70    IF PD<0 .OR. PD>180 THEN GOTO 50
80    IF F1 < 30 THEN R = 0: PRINT "SET ROT. SW. ON SIDE PANEL TO POS. 1"
90    IF F1>=30 .AND. F1<65 THEN R=1 :PRINT "SET ROT. SW. ON SIDE PANEL TO 2"
100   IF F1>=65 .AND. F1<140 THEN R=2:PRINT "SET ROT. SW. ON SIDE PANEL TO 3"
110   IF F1>=140 .AND. F1<315 THEN R=3:PRINT "SET ROT.SW. ON SIDE PANEL TO 4"
120   IF F1>=315 .AND. F1<655 THEN R=4:PRINT "SET ROT.SW. ON SIDE PANEL TO 5"
130   PRINT "WHEN DONE, PRESS ANY NUMBER AND C/R :"
140   INPUT TEMP
REM   ACQUIRE LOWER (LF0) AND HIGHER (HF1) FREQ. LIMITS FOR GIVEN SW. POS.
145   DATA 15,32,30,65,64,140,137,315,303,655
150   FOR I = 1 TO R + 1
160   READ LF0, HF1
170   NEXT I
175   PRINT "LOWER FREQ. LIMIT = ", LF0
180   PRINT "UPPER FREQ. LIMIT = ", HF1
REM   FOR FREQ. VARYING FROM LF0 TO HF1, THE DIGITAL VALUE FOR PD=0 HAS TO
REM   VARY FROM 135 TO 254; AND FOR PD=180, IT IS 93 TO 153.
REM   HENCE FIND TOTAL RANGE FOR PD=0 (LRP) AND FOR PD=180 (HRP)
190   LRP = 254 - 135: HRP = 153 - 93
REM   FIND TOTAL ANALOG FREQ. RANGE (DFR), & THE DIFFERENCE OF THE ACTUAL
REM   FREQUENCY FROM THE LOWER (LDFR) AND THE UPPER LIMITS (HDFR).
200   DFR = HF1 - LF0: LDFR = F1 - LF0: HDFR = HF1 - F1
REM   USING LINEAR (ANALOG FREQ. v/s DIGITAL PHASE DELAY), FIND CORRESPONDING
REM   LOWER (LP FOR PD=0) AND HIGHER (HP FOR PD =180) DIGITAL PHASE DELAY
REM   LIMITS FOR THE GIVEN FREQUENCY F1.
210   LP = INT((135 + LDFR * LRP / DFR) + .5)
220   HP = INT((153 - HDFR * HRP / DFR) + .5)
REM   FIND TOTAL TIME PERIOD T; ACTUAL TIME T1 FOR PHASE DELAY PD.
230   T = 1 / F1: T1 = PD * T / 360
REM   FIND TOTAL DIGITAL VALUE VARIATION (PDFR) FROM 0 TO 180, FOR FREQ. F1.
240   PDFR = LP - HP
REM   PDFR IS THE DIGITAL PHASE DELAY VARIATION FOR PERIOD T.
REM   USING LINEAR (PDFR v/s TIME), FIND ACTUAL DIGITAL VALUE
REM   FOR THE GIVEN PHASE DELAY PD
250   DGV = LP - (2 * PDFR * T1 / T)
REM   FOLLOWING FN. GIVES A BETTER APPROXIMATION (AMPL. OF SINE TERM CAN
REM   BE CHANGED AS DESIRED); ARGUMENT IS IN RADIANS.
255   D1 = DGV - ABS(15 * SIN(PD * PI / 180))
257   PRINT "DIGITAL VALUE OF PHASE DELAY = ", D1
REM   OUTPUT D1 TO CORRESPONDING DATA LATCH
260   FOR I = 1 TO 2
270   XBY(25000) = 0
280   PORT1 = D1
290   XBY(15000) = 0
300   NEXT I
310   STOP
320   END
```

```
REM     (SIMP_FSW.BAS)          ... RAJIV K. BAPHNA  ; DEC. 1990
REM     THIS PROGRAM OUTPUTS A SW. FREQ. WHICH IS THE SUM OR
REM     DIFFERENCE OF THE INPUT AND OUTPUT FREQUENCIES.
150     PRINT "FIN +/- FOUT SHOULD LIE BETWEEN 5-1450 Hz."
160     PRINT "ENTER INPUT FREQUENCY :"
170     INPUT FIN
172     IF FIN < 0 THEN 160
175     PRINT "ENTER REQD. OUTPUT FREQUENCY :"
177     INPUT FOUT
179     IF FOUT < 0 THEN 175
180     PRINT "DO YOU WANT SUM (1) OR DIFFERENCE (2) ?"
184     INPUT B1
185     IF B1 = 2 THEN FR = ABS(FIN - FOUT): GOTO 195
187     IF B1 = 1 THEN FR = FIN + FOUT: GOTO 195
190     GOTO 180
195     IF FR < 5 .OR. FR > 1450 THEN 150
200     F1 = INT(FR)
REM     DEPENDING ON FREQ., SET MARKERS TO BRANCH TO APPROPRIATE SUBRTS.
210     IF F1 <= 12 THEN R = 0
220     IF F1<=150 .AND. F1>12 THEN R=1
230     IF F1 > 150 THEN R = 2
240     ON R GOSUB 2000, 3000, 4000
REM     LATCH DIGITAL VALUE OF FREQ. (DF1)
250     FOR I = 1 TO 2
260     XBY(19000) = 0
270     PORT1 = DF1
280     XBY(15000) = 0
290     NEXT I
410     STOP
2000    PRINT "SET FREQ. ROT. SW. ON BACK PANEL TO POSITION 1"
2010    PRINT "WHEN DONE, PRESS ANY NUMBER AND C/R :"
2020    INPUT TEMP
2040    IF F1 <= 8 THEN MAX = 230 ELSE MAX = 235
REM     ACTUAL FREQ. RANGE POSSIBLE FOR THIS SW. POS. IS 2.5 TO 12 Hz.,
REM     I.e., ABOUT 9  Hz. (FOR A DIGITAL RANGE OF 225 TO 147,I.e., 78.
REM     ASSUMING LINEAR (ANALOG FR. RANGE v/s DIG. FREQ. RANGE),
REM     FIND DIGITAL VALUE (DF1) FOR GIVEN FREQUENCY F1.
2050    DF1 = INT(MAX - (78 / 9) * (F1 - 2.5))
2100    RETURN
3000    PRINT "SET FREQ. ROT. SW. ON BACK PANEL TO POSITION 2"
3010    PRINT "WHEN DONE, PRESS ANY NUMBER AND C/R :"
3020    INPUT TEMP
3040    IF F1 <= 30 THEN MAX = 238
3050    IF F1>30 .AND. F1<=74 THEN MAX=240
3060    IF F1>74 .AND. F1<=130 THEN MAX=242
3070    IF F1 > 130 THEN MAX = 246
REM     SAME LOGIC AS DESCRIBED FOR ROT. SW. POS. 1.
REM     ACTUAL FREQ. RANGE 8 TO 150 Hz. (DIG. RANGE 237 TO 150)
3080    DF1 = INT(MAX - (87 / 142) * (F1 - 8))
3130    RETURN
4000    PRINT "SET FREQ. ROT. SW. ON BACK PANEL TO POSITION 3"
4010    PRINT "WHEN DONE, PRESS ANY NUMBER AND C/R :"
4020    INPUT TEMP
4040    IF F1 < 154 THEN F1 = 154
4050    IF F1 < 935 THEN MAX = 235: MIN = 154: DN = 30
4060    IF F1 >=935 .AND. F1<=1047 THEN MAX=209:MIN=935:DN=20
4070    IF F1 > 1047 THEN MAX = 199: MIN = 1020: DN = 8
```

```
REM     SAME LOGIC AS DESCRIBED FOR ROT. SW. POS. 1
REM     DIFF. CONSTS. FOR DIFF. RANGES OF FREQ. ARE GIVEN IN MIN. AND DN.
4080    DF1 = INT((MAX - (F1 - MIN) / DN) + .5)
4130    RETURN
5000    END
```

```
REM     (PWM.BAS)              ... RAJIV K. BAPHNA  ;  DEC. 1990
REM     THIS PROGRAM PERFORMS OPEN-LOOP SINUSOIDAL PWM.
REM     FOLLOWING IS A LOOK-UP TABLE FOR CONSTANT AMPL. INTEGR. :
REM     ARRAY A CONTAINS REQD. GAINS FOR CONST. AMPL. TRIANGLE WAVE
REM     AFTER INTEGR. (ROT. SW. POS. 1) FOR FREQ. RANGE 0-12 Hz.
REM     THE CORRESP. DIG. FREQ. VALUES ARE 150-200 (STEPS OF 10) & 208.
REM     SIMILARLY ARRAY B IS FOR ROT SW. POS. 2 (13-150 Hz.); DIG. FREQ.
REM     VALUES ARE 150-230 (STEPS OF 10).
REM     ARRAY C IS FOR ROT. SW. POS. 3 (151-1450 Hz.); DIG. FREQ. VALUES
REM     ARE 160-220 (STEPS OF 10), AND 221-235 (STEPS OF 1).
REM     OTHER GAINS FOR INTERMEDIATE FREQS. ARE LINEARLY INTERPOLATED.
10      DIM A(6), B(9), C(22)
20      FOR I = 1 TO 6
30      READ A(I)
40      NEXT I
50      FOR I = 1 TO 9
60      READ B(I)
70      NEXT I
80      FOR I = 1 TO 22
90      READ C(I)
100     NEXT I
110     DATA 140,150,160,180,210,240
120     DATA 28,30,34,40,45,54,73,100,180
130     DATA 24,28,32,34,36,38,55,60,65,68,70,75,80,85,90,98,105
140     DATA 120,130,140,165,190
150     PRINT "SINUSOIDAL PWM CONVERTER"
160     PRINT "ENTER INPUT VOLTAGE :"
170     INPUT VIN
175     PRINT "ENTER O/P VOLTAGE AMPLITUDE ( <=VIN ) :"
177     INPUT VO
178     IF VO > VIN THEN GOTO 175
180     PRINT "ENTER REQD. O/P FREQUENCY (BET. 5 & 1450 Hz. ONLY) :"
190     INPUT FR
195     IF FR < 5 .OR. FR > 1450 THEN 180
200     F1 = INT(FR)
REM     DEPENDING ON FREQ., SET MARKERS TO BRANCH TO APPROPRIATE SUBRTS.
210     IF F1 <= 12 THEN R = 0
220     IF F1<=150 .AND. F1>12 THEN R=1
230     IF F1 > 150 THEN R = 2
240     ON R GOSUB 2000, 3000, 4000
REM     LATCH DIGITAL VALUE OF FREQ. (DF1)
250     FOR I = 1 TO 2
260     XBY(19000) = 0
270     PORT1 = DF1
280     XBY(15000) = 0
290     NEXT I
REM     LATCH DIGITAL VALUE OF APPROPRIATE GAIN FOR TRIANGLE WAVE
300     FOR I = 1 TO 2
310     XBY(21000) = 0
320     PORT1 = GAIN
330     XBY(15000) = 0
340     NEXT I
REM     FIND APPROPRIATE GAIN FOR FINAL SINE WAVE (MOD. FN.).
REM     CHANGE MAX. AMPL. AS DESIRED, IN THE FOLLOWING FN.
REM     ASSUME LINEAR (ANALOG VOLTAGE v/s DIGITAL VALUE).
REM     LATCH THE DIGITAL VALUE FOR GAIN (DA1).
350     DA1 = INT(200 * VO / VIN + .5)
```

```
360     FOR I = 1 TO 2
370     XBY(23000) = 0
380     PORT1 = DA1
390     XBY(15000) = 0
400     NEXT I
410     STOP
2000    PRINT "SET FREQ. ROT. SW. ON BACK PANEL TO POSITION 1"
2010    PRINT "WHEN DONE, PRESS ANY NUMBER AND C/R :"
2020    INPUT TEMP
2040    IF F1 <= 8 THEN MAX = 230 ELSE MAX = 235
REM     ACTUAL FREQ. RANGE POSSIBLE FOR THIS SW. POS. IS 2.5 TO 12 Hz.,
REM     I.e., ABOUT 9  Hz. (FOR A DIGITAL RANGE OF 225 TO 147,I.e., 78.
REM     ASSUMING LINEAR (ANALOG FR. RANGE v/s DIG. FREQ. RANGE),
REM     FIND DIGITAL VALUE (DF1) FOR GIVEN FREQUENCY F1.
2050    DF1 = INT(MAX - (78 / 9) * (F1 - 2.5))
REM     FIX APPROPRIATE GAIN FOR TRIANGLE WAVE
REM     SINCE LOOK-UP TABLE FROM 200 TO 208 IS NOT CONSISTENT WITH
REM     PREVIOUS VALUES, ITS GAIN IS INTERPOLATED AS FOLLOWS :
REM     254-240=14 ; 208-200=8.
2060    IF DF1 > 200 THEN GAIN = INT((DF1 - 200) * 14 / 8 + 240): RETURN
REM     FOR OTHER VALUES OF DF1 :
REM     CHECK IF DF1 IS A MULTIPLE OF 10; IF NOT, INTERPOLATE LINEARLY.
2070    N = (DF1 - 140) / 10
2080    N1 = INT(N): N2 = (N - N1) * 10: DFR = (A(N1 + 1) - A(N1))
2090    IF N = N1 THEN GAIN = A(N1) ELSE GAIN = (DFR * N2 / 10) + A(N1)
2100    RETURN
3000    PRINT "SET FREQ. ROT. SW. ON BACK PANEL TO POSITION 2"
3010    PRINT "WHEN DONE, PRESS ANY NUMBER AND C/R :"
3020    INPUT TEMP
3040    IF F1 <= 30 THEN MAX = 238
3050    IF F1>30 .AND. F1<=74 THEN MAX=240
3060    IF F1>74 .AND. F1<=130 THEN MAX=242
3070    IF F1 > 130 THEN MAX = 246
REM     SAME LOGIC AS DESCRIBED FOR ROT. SW. POS. 1.
REM     ACTUAL FREQ. RANGE 8 TO 150 Hz. (DIG. RANGE 237 TO 150)
3080    DF1 = INT(MAX - (87 / 142) * (F1 - 8))
3090    IF DF1 > 230 THEN GAIN = INT((DF1 - 230) * 74 / 4 + 180): RETURN
3100    N = (DF1 - 140) / 10
3110    N1 = INT(N): N2 = (N - N1) * 10: DFR = (B(N1 + 1) - B(N1))
3120    IF N = N1 THEN GAIN = B(N1) ELSE GAIN = (DFR * N2 / 10) + B(N1)
3130    RETURN
4000    PRINT "SET FREQ. ROT. SW. ON BACK PANEL TO POSITION 3"
4010    PRINT "WHEN DONE, PRESS ANY NUMBER AND C/R :"
4020    INPUT TEMP
4040    IF F1 < 154 THEN F1 = 154
4050    IF F1 < 935 THEN MAX = 235: MIN = 154: DN = 30
4060    IF F1 >=935 .AND. F1<=1047 THEN MAX=209:MIN=935:DN=20
4070    IF F1 > 1047 THEN MAX = 199: MIN = 1020: DN = 8
REM     SAME LOGIC AS DESCRIBED FOR ROT. SW. POS. 1
REM     DIFF. CONSTS. FOR DIFF. RANGES OF FREQ. ARE GIVEN IN MIN. AND DN.
4080    DF1 = INT((MAX - (F1 - MIN) / DN) + .5)
REM     FOR DF1 > 220, ALL VALUES OF REQD. GAIN ARE IN LOOK-UP TABLE.
4090    IF DF1 > 220 THEN N = DF1 - 220 + 7: GAIN = C(N): RETURN
4100    N = (DF1 - 150) / 10
4110    N1 = INT(N): N2 = (N - N1) * 10: DFR = (C(N1 + 1) - C(N1))
4120    IF N = N1 THEN GAIN = C(N1) ELSE GAIN = (DFR * N2 / 10) + C(N1)
4130    RETURN
```

```
REM     STOP PROGRAM RUN AND TERMINATE
5000    END
```

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